nexperia

ESD in Automotive In-Vehicle Networks

SE IEEE EMC Society

Q2 2021

Nexperia‘s Contacts for ESD Protection

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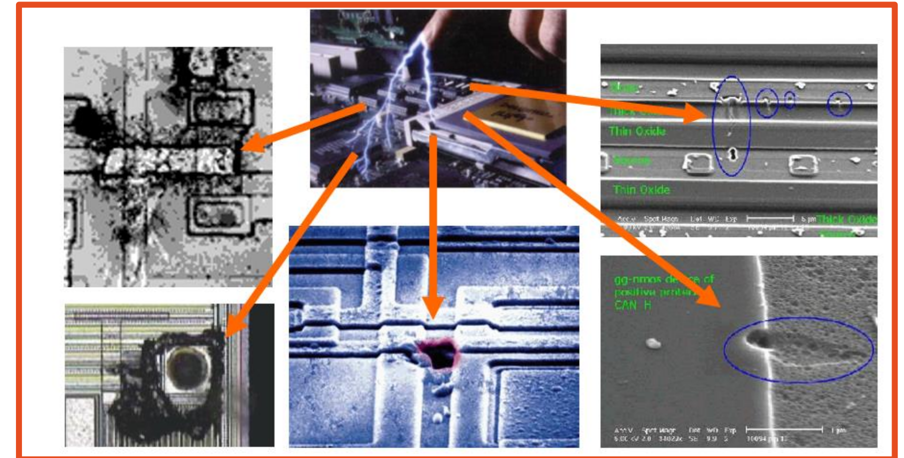
Overview

- **Motivation**
- **Datasheet Parameters and Selection Criteria for ESD Protection Devices**
- **ESD protection for**
  - Classics: LIN/CAN, CAN-FD
  - Automotive Ethernet (OPEN Alliance)
  - High Speed Links
- **Extra: How to simulate ESD?**

ESD – Electro Static Discharge

WHAT

A sudden electrostatic discharge between persons, devices or components



HOW

- A charged person touches an integrated circuit (IC)
- A charged IC drops on a grounded metal plate
- A charged machine touches an IC
- An electrostatic field is induced by high voltages

PROBLEM

- Causing malfunction (**reversible** by power-off-on cycle)
- Destruction of electrical components (**irreversible**): gate oxide, metallisation or PN junctions

ESD – Electro Static Discharge

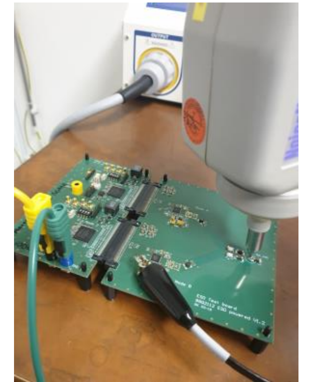
Device level

- **ICs can be destroyed (ESD) during production (assembly, placement, handling)**
- Qualification by standards (JEDEC)
  - **Human Body Model (HBM), 2kV for IC pins**
  - Machine Model (MM)
  - Charged Device Model (CDM)

- ESD pulses are given to all IC pins.
- ESD "on-chip protection" protects against defects during production.

System level

- Complete Systems (e.g. clusters, head units) can be destroyed by ESD during operation or service
- "System Level" ESD standards
  - **IEC 61000-4-2**
    Electrostatic discharge immunity test
  - ISO 10605

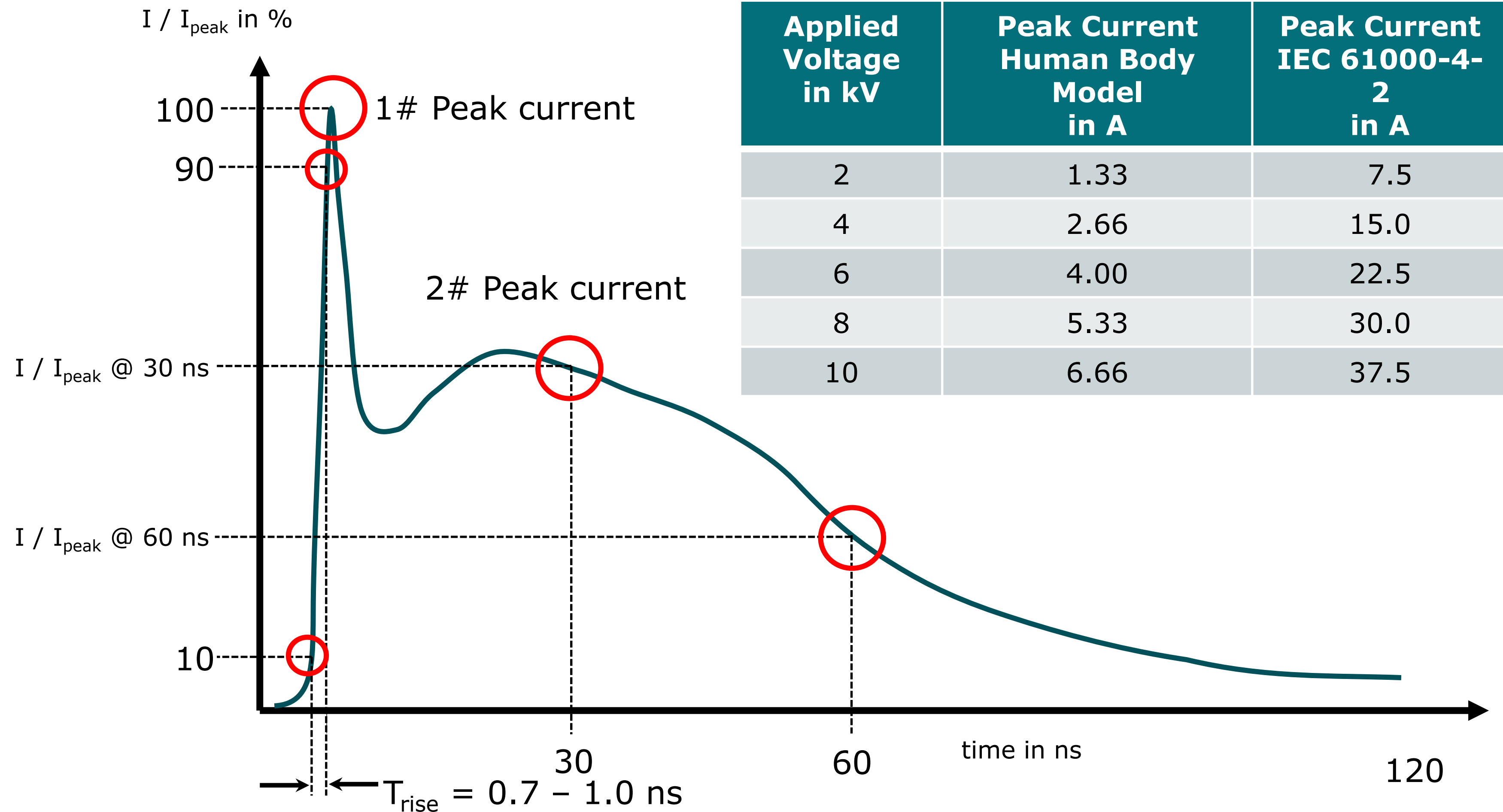


- ESD pulses are given to certain accessible interfaces.
  Individual components (e.g. ICs) are not tested!
- Special ESD Devices are added on the board to avoid destruction by ESD.

ESD – System Level Testing: IEC 61000-4-2

Typical waveform of ESD current

- Rise time
  - 0.7 – 1 ns
    (von 10% auf 90%)
- Peak current
  - +/- 10% tolerance
- Current after 30 ns
  - +/- 30% tolerance
- Current after 60 ns
  - +/- 30% tolerance

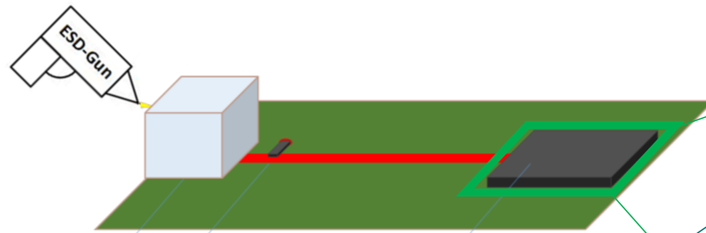


Applied Voltage in kV	Peak Current Human Body Model in A	Peak Current IEC 61000-4-2 in A
2	1.33	7.5
4	2.66	15.0
6	4.00	22.5
8	5.33	30.0
10	6.66	37.5

System ESD Testing

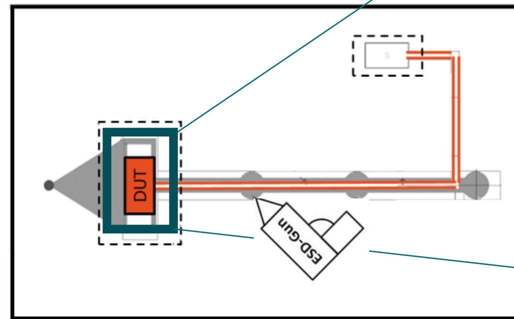
Direct (contact) discharge:

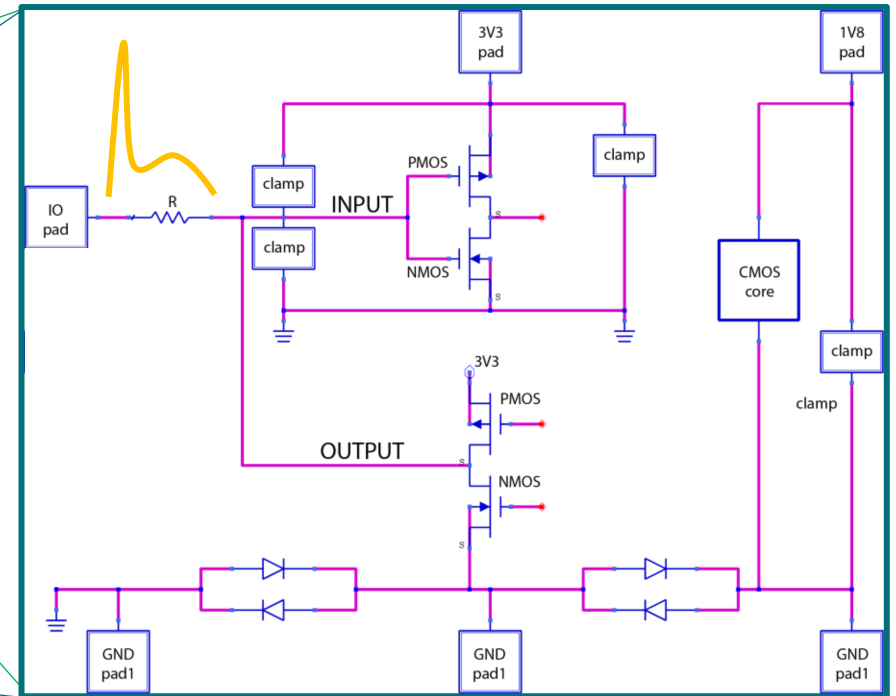
6 to 15kV



Indirect discharge

≥15kV



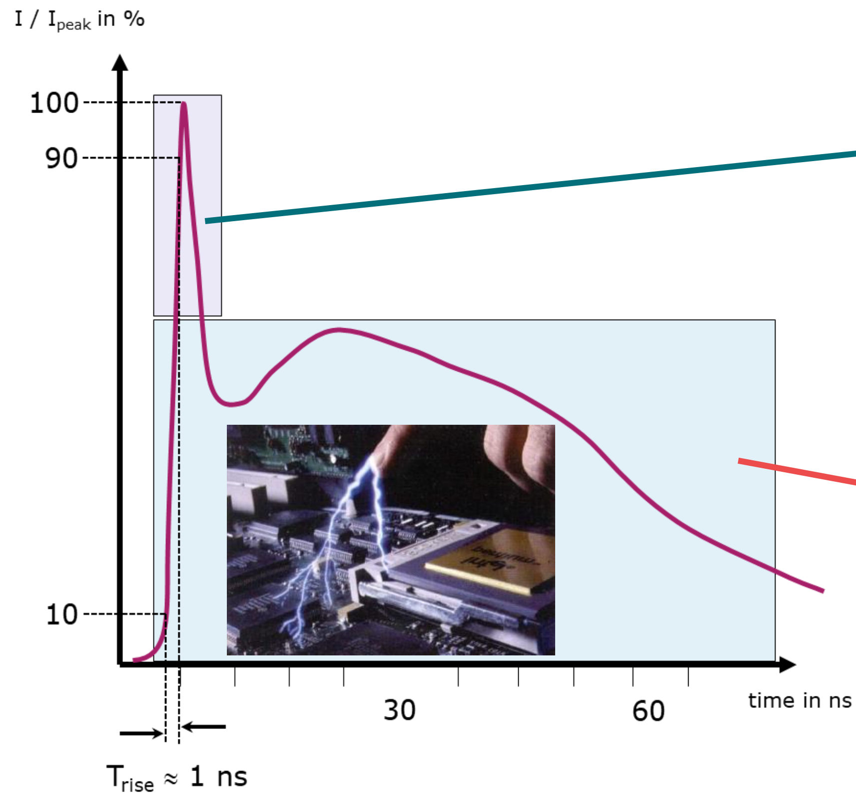


Air discharge

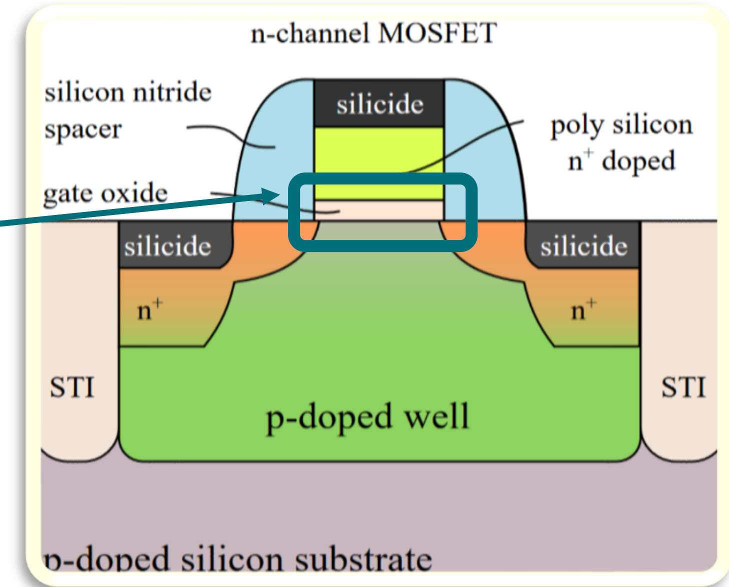
Strongly dependent on the system.

ESD – Defects caused by ESD

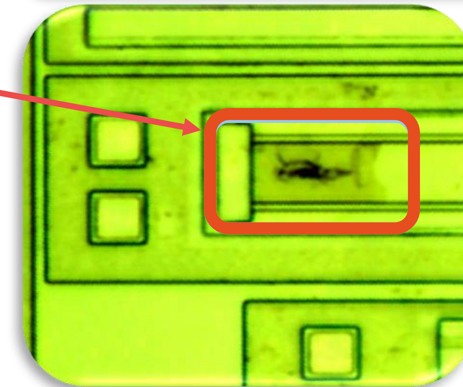
Destruction mechanism



High voltage

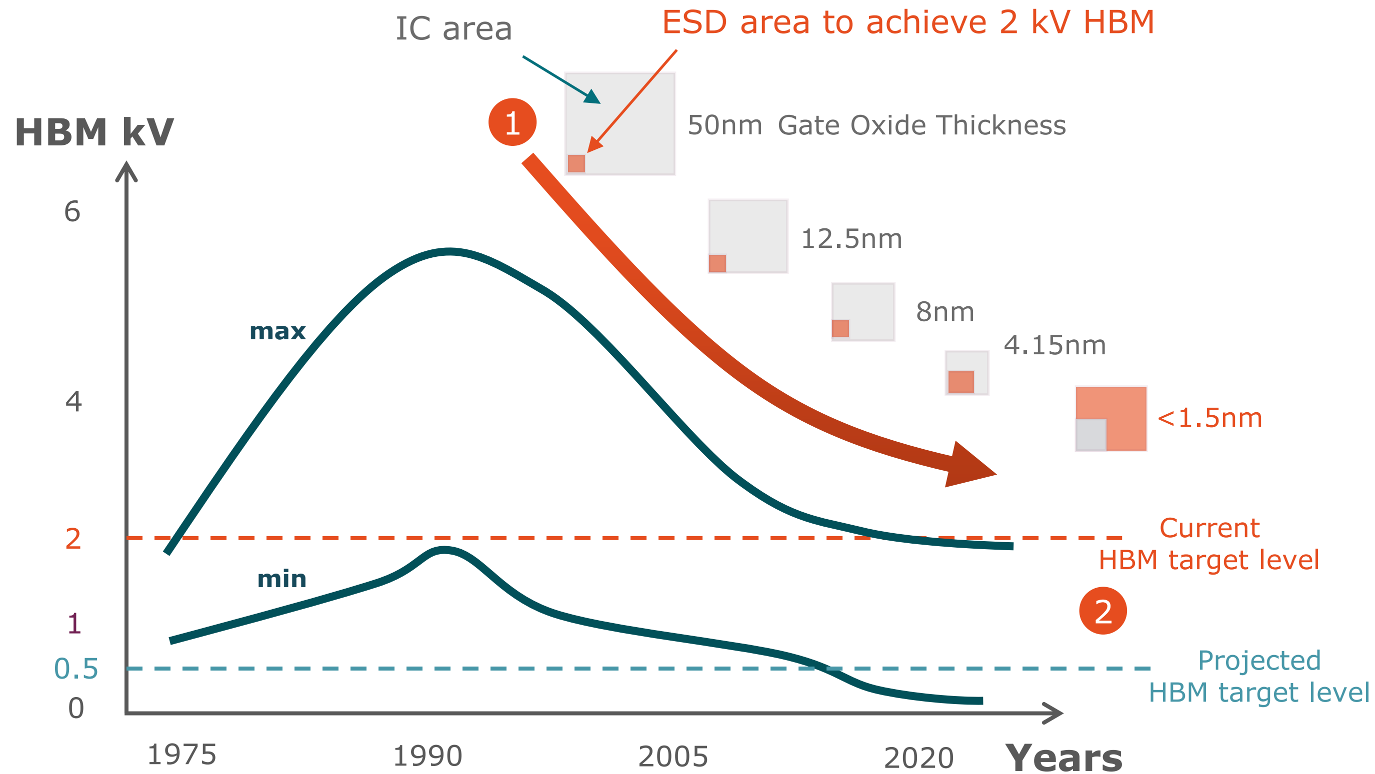


High energy



ICs become more sensitive

Increased performance and density lower the SoC ESD robustness



Source:
ESDA, 2016
Duvvy/Miller, 2009

1 **ICs becoming more sensitive**

- Gate thickness and chip size (channel length) decreases
- Maximum gate voltage decreases (e.g. for CMOS090 <1.5V static)
- New Processes are optimized for area and performance

2 **HBM targets will be lowered**

- HBM targets will be lowered to meet device level ESD robustness
- HBM target already lowered down to 1 kV
- This trend is applicable for **CDM targets**

IC robustness will decrease and require more dedicated discrete ESD solutions

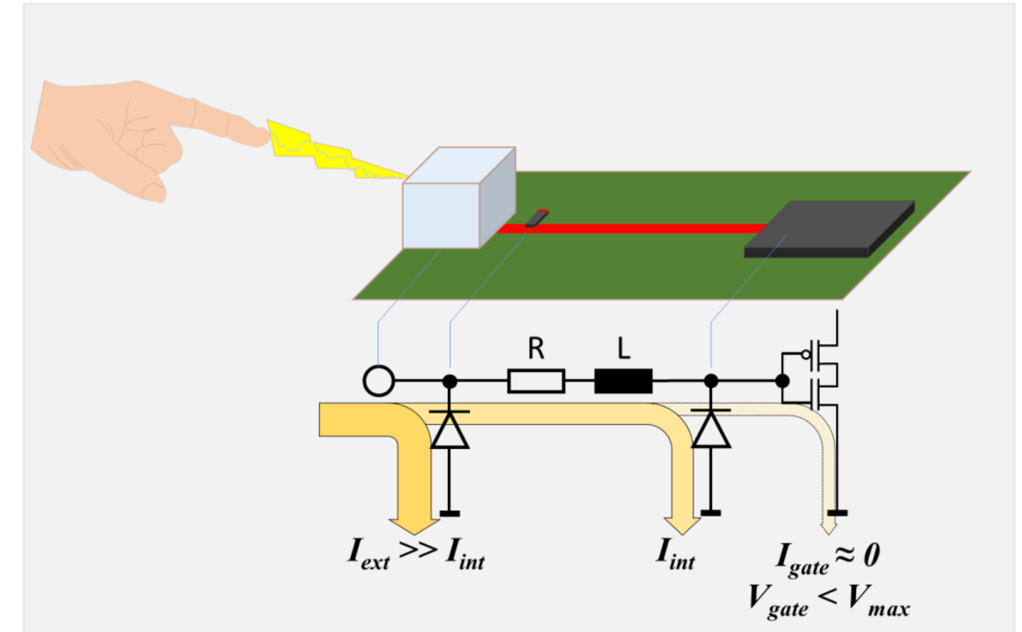
public

Benefits of external ESD protection

Example CAN bus with PESD2IVN24-T

Device level | System level

IC/Transceiver	ESD robustness w/o	ESD robustness with PESD2IVN24-T
TLE 9263BQXV33XUMA1	+ 8 kV (HBM)	+ 30 kV
TLE 9262BQXXUMA1	+ 8 kV (HBM)	+ 30 kV
MCP25625 E/SS	+ 8 kV (HBM)	+ 30 kV
LPC11C22FBD48/301	+ 8 kV (HBM)	+ 30 kV
SN65HVD232QDRQ1	+ 11 kV (HBM)	+ 30 kV
TLE7250GXUMA1	+ 10 kV (HBM)	+ 30 kV
TJA1042T/3,118	+ 12 kV (HBM)	+ 30 kV
TJA1044T	+ 10 kV (HBM)	+ 30 kV
⋮	⋮	+30 kV



External ESD Protection can handle **more ESD current** and can be chosen **application specific**.

Very Robust System in the Field!

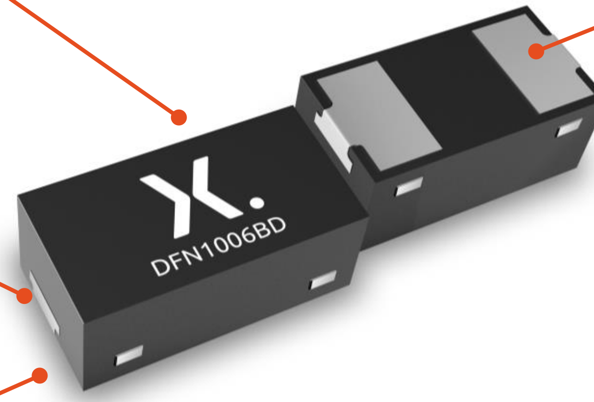
Selection Criterion

Package (shape/size/footprint)

Side-wettable flanks for AOI

Number of signal lines

e.g. differential or single ended, one or more channels

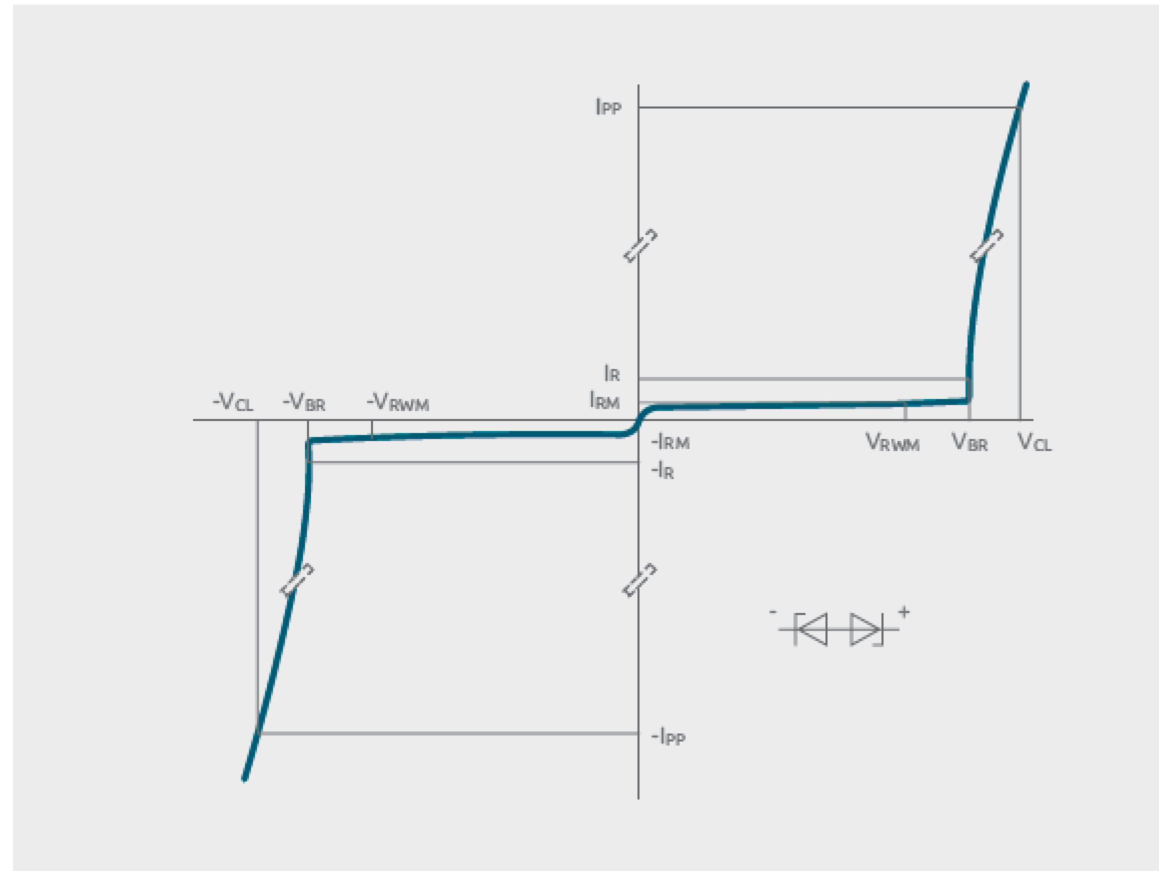


Electrical performance

- Reverse stand-off voltage V_{RWM}
- Breakdown or trigger voltage V_{br} or V_t
- Clamping voltage V_{clamp}
- Dynamic resistance R_{dyn}
- **Device capacitance C_d** and other parasitics

Characteristics of ESD Protections

Classical Zener Characteristic



V_{RWM}: Reverse standoff voltage
V_{BR}: Breakdown voltage
V_{CL}: Clamping voltage
I_{RM}: Maximum reverse current
I_{PP}: Maximum surge current

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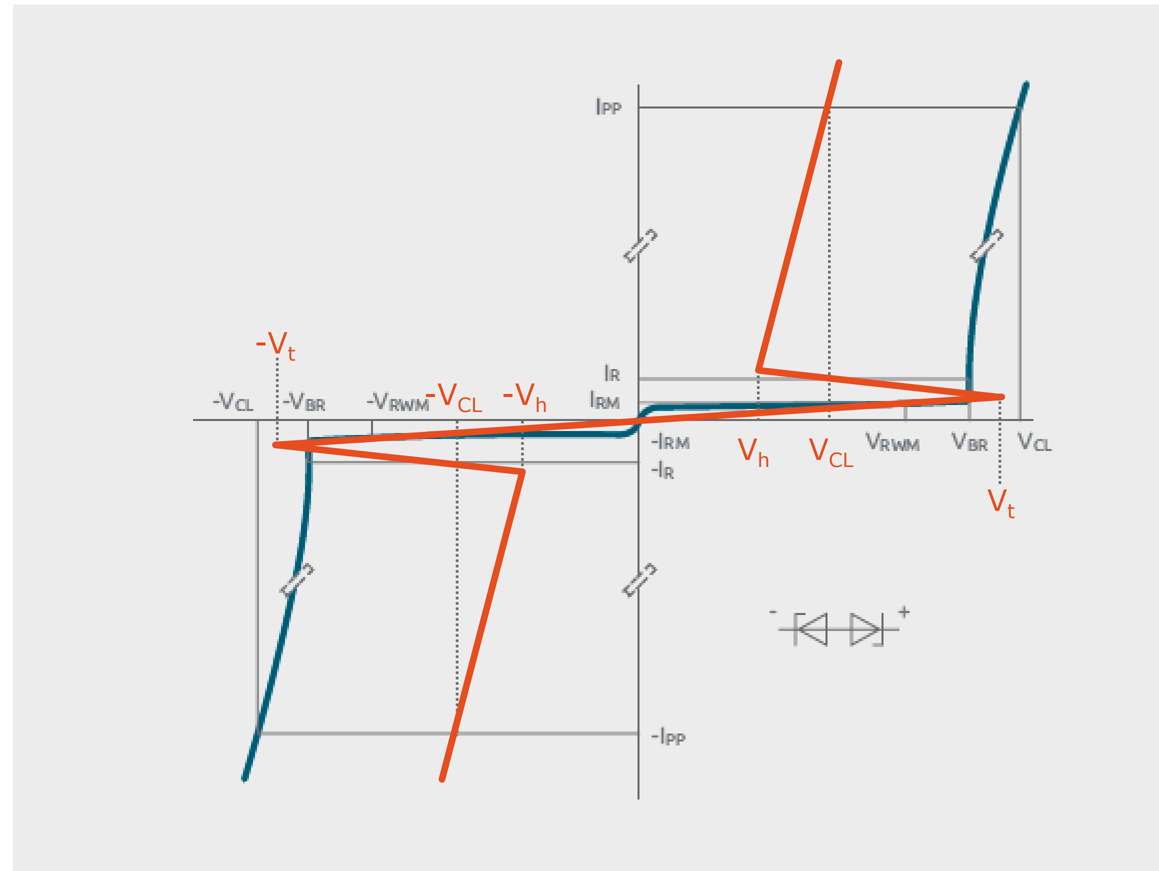
Characteristics of new ESD Protections

Snap Back



V_{RWM}: Reverse standoff voltage
V_{BR}: Breakdown voltage
V_{CL}: Clamping voltage
I_{RM}: Maximum reverse current
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V_t: Trigger voltage
V_h: Holding voltage

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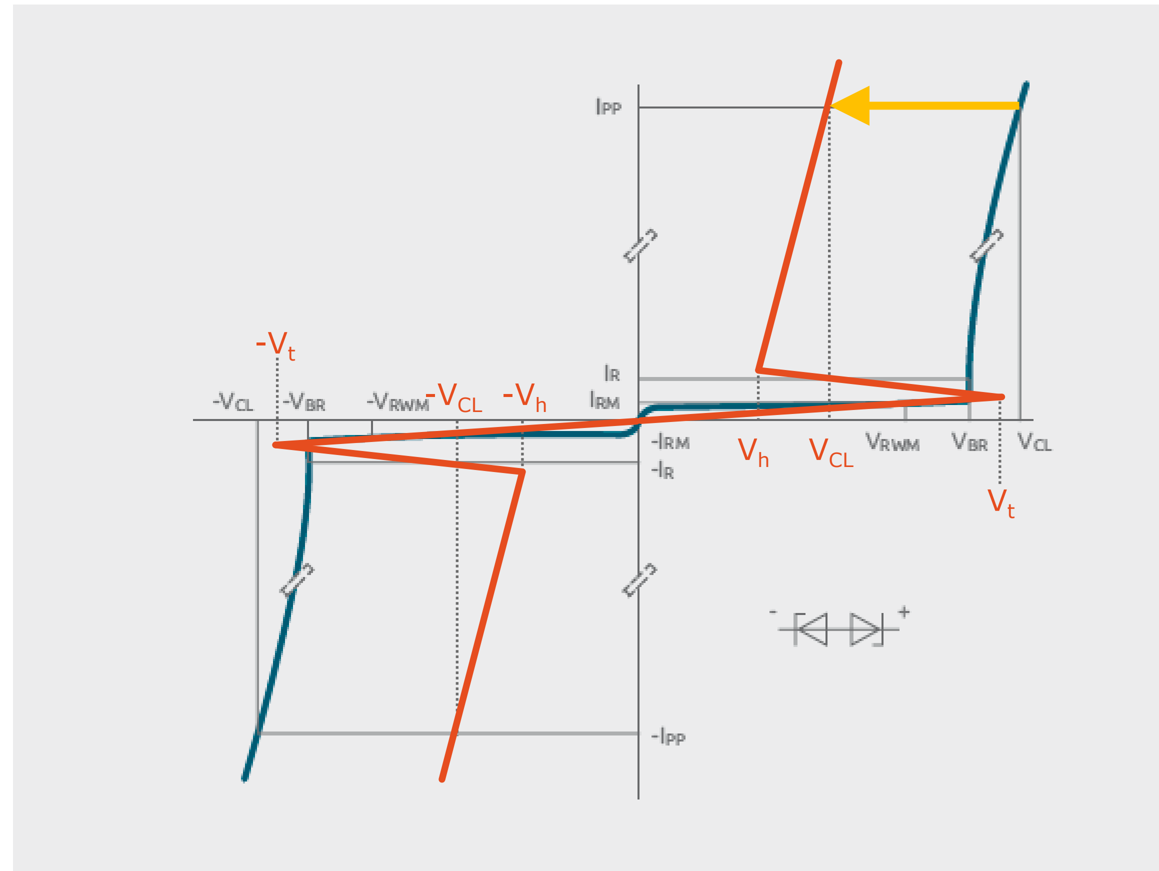

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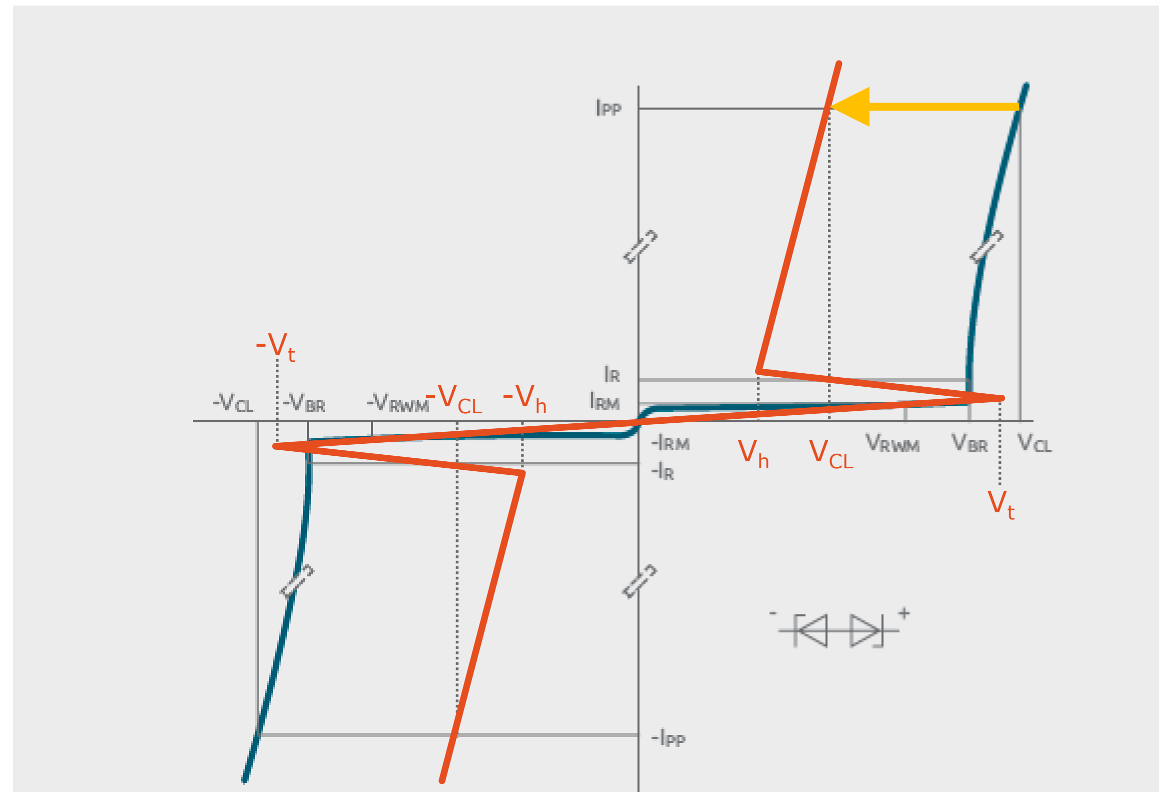

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V_h: Holding voltage

Reducing V_{CL} -> Improving Robustness of the PHY

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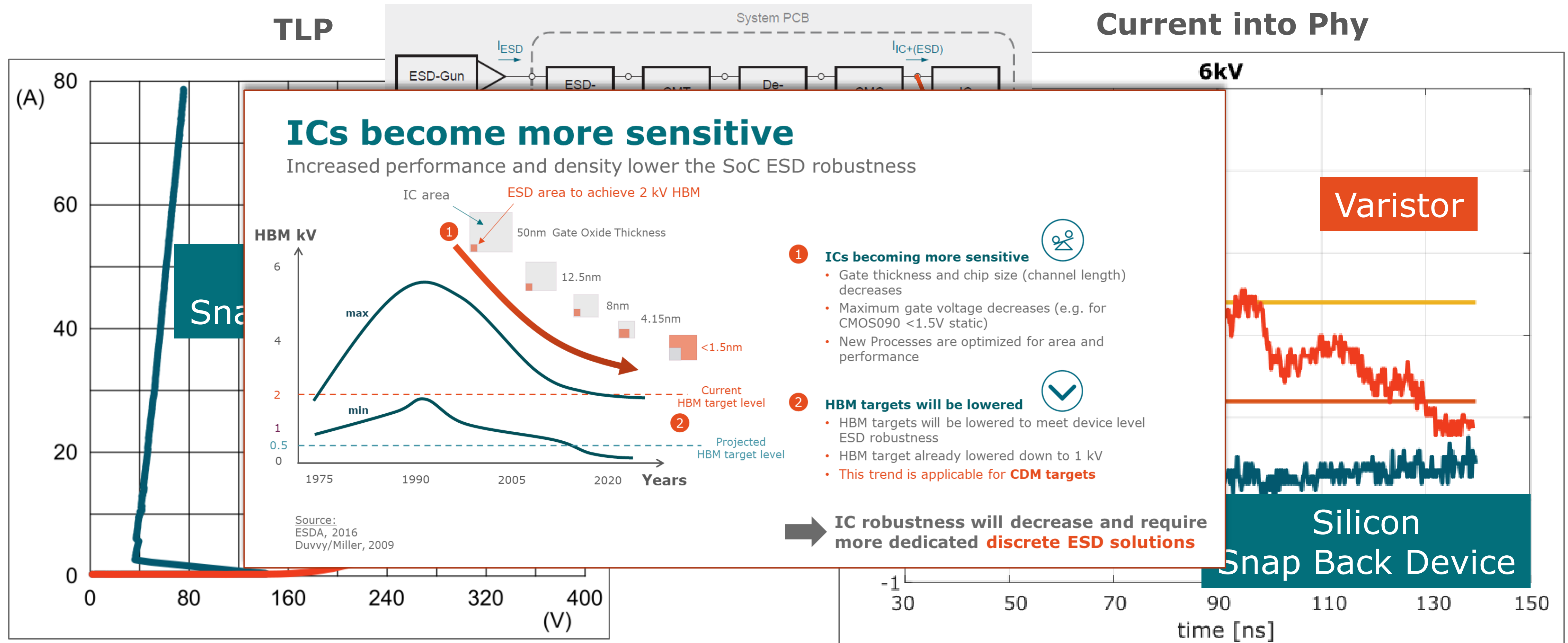
Example: Automotive Ethernet

Clamping performance and system robustness



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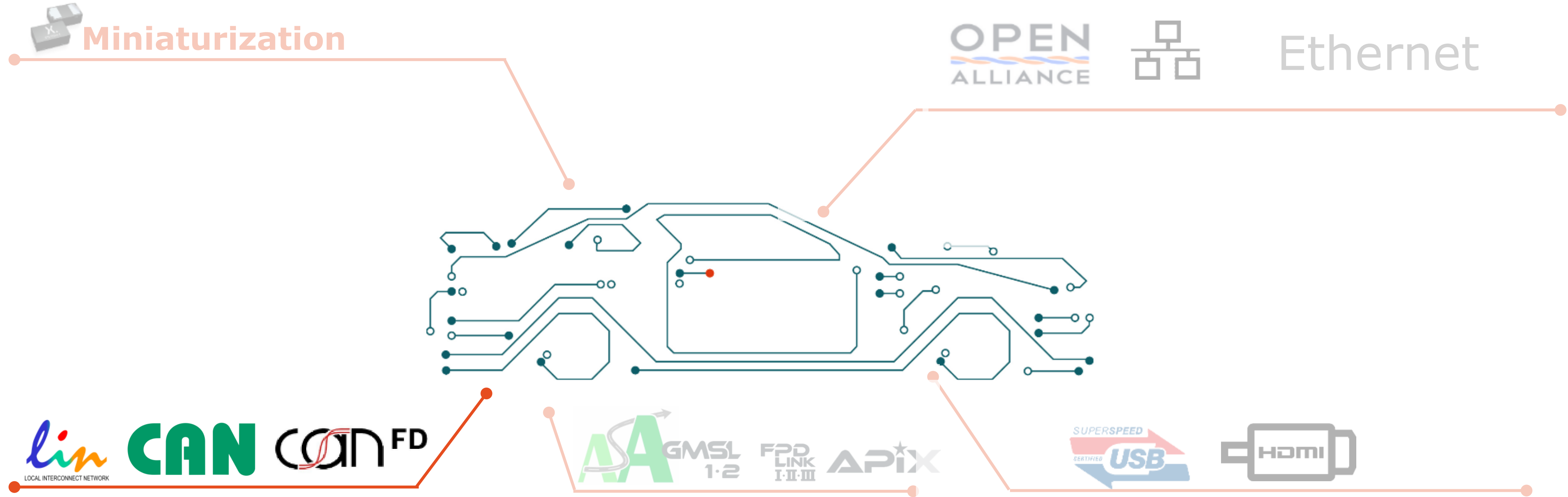
Automotive ESD Protection



LIN/CAN

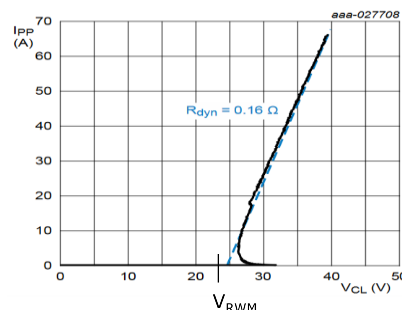
- Requirement for ESD protection depend on OEM (approval list)

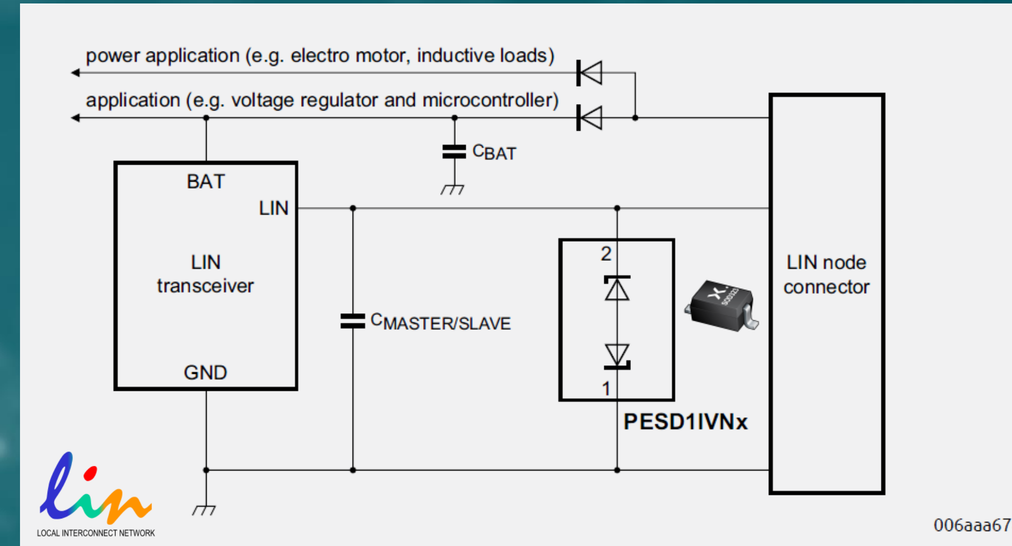
->Emission and Immunity: DPI, Pulses, ESD

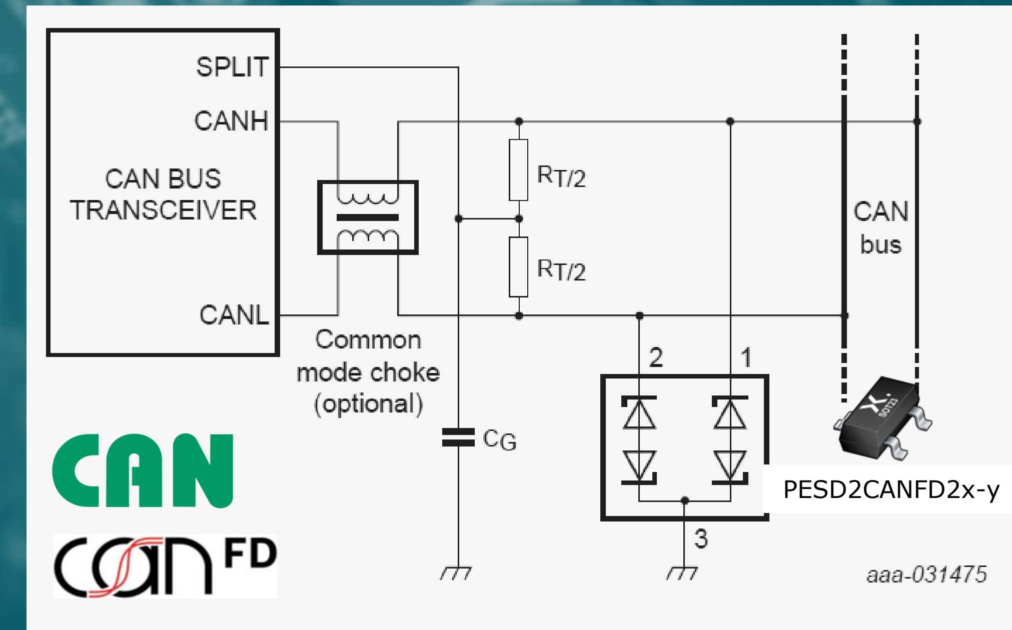
(in combination with transceiver!)

- Common requirements:

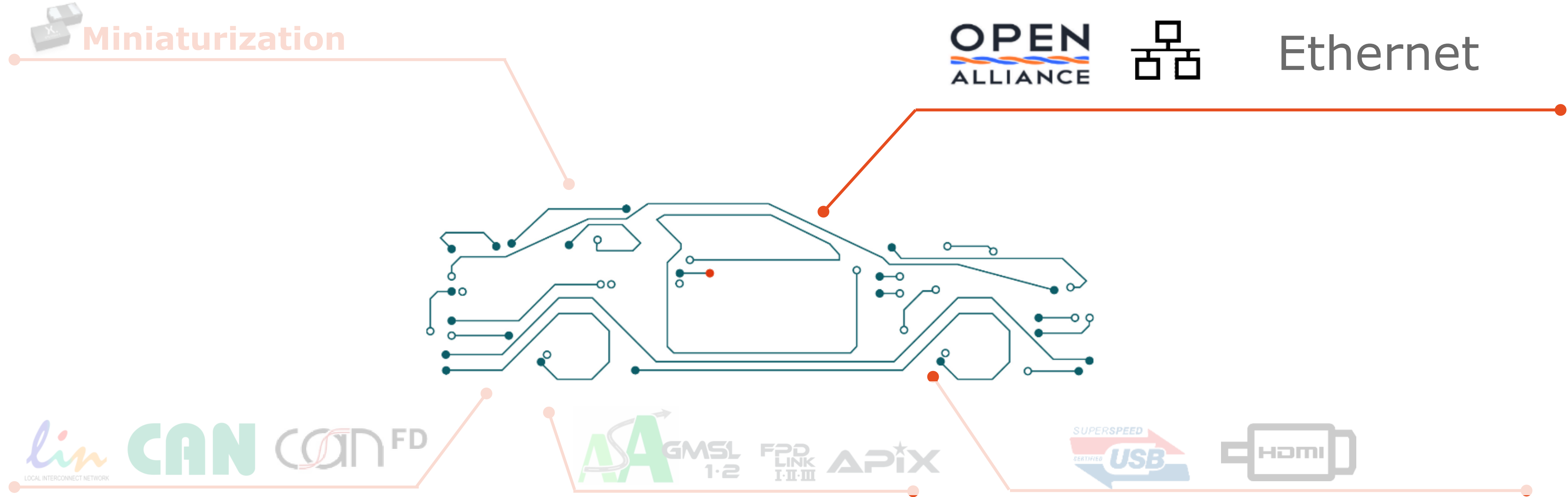
	LIN	CAN HS	CAN FD
Cd	30 … 100pF	10 … 30pF	3.5 … 10 (30) pF
ΔCd/Cd	nA	typical < 0.5% for modern devices	
V_{RWM}	12 V Board Net		24 V Board Net
	>24V ISO16750-2 (28V)		>32V ISO16750-2



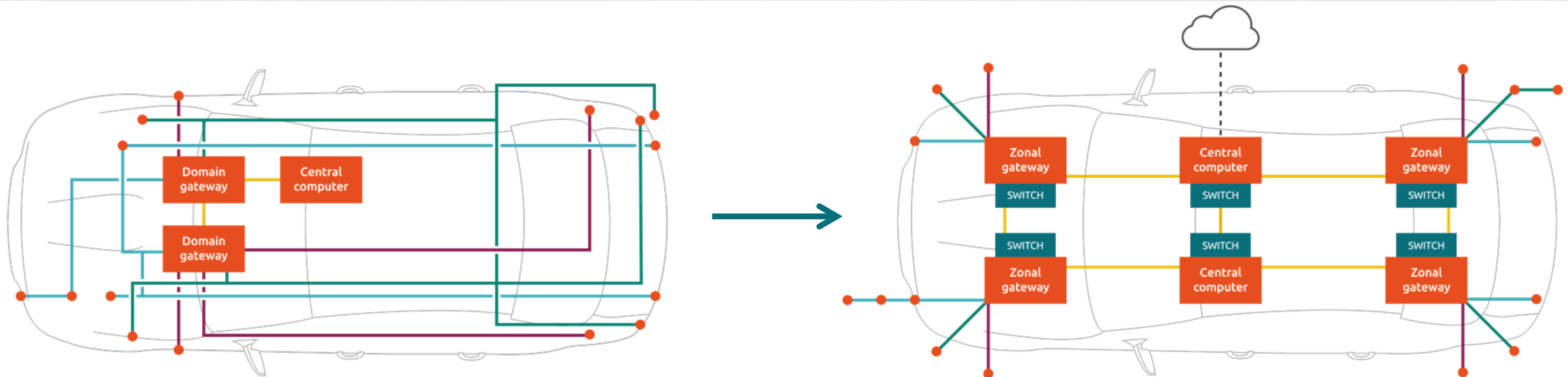




Automotive ESD Protection

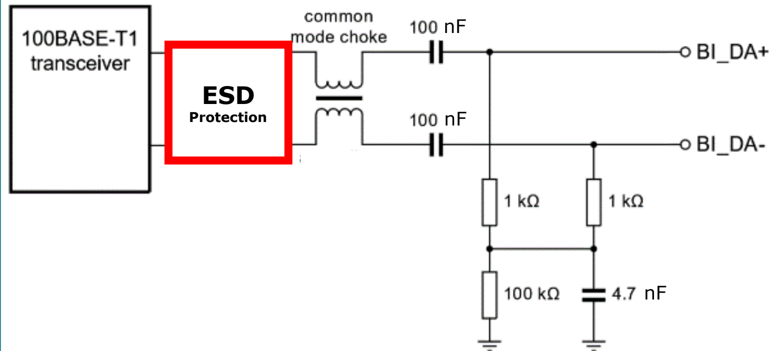


Evolution of In-Vehicle Networking



Classic Ethernet vs. OPEN Alliance

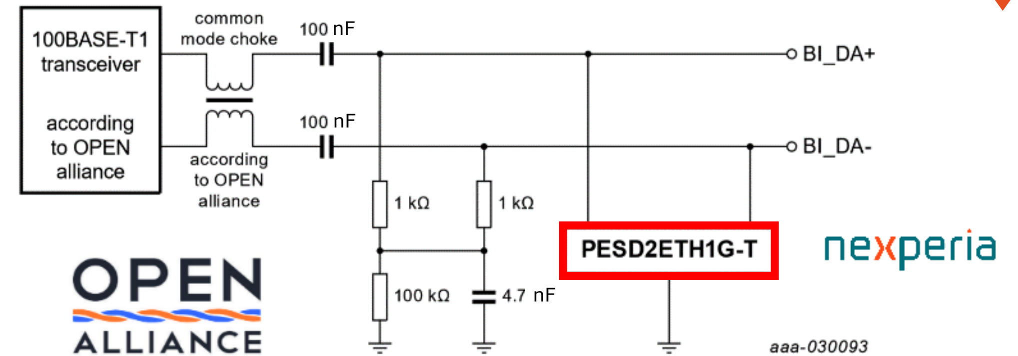
Classic Ethernet



ESD Protection behind DC block, CMC and in front of PHY

- **Dual sourcing of ESD protection critical**, because TLP curves and turn on behaviour need to match
- Internal protection of the PHY and external ESD protection cannot always be matched

OPEN Alliance Ethernet



ESD Protection in front of DC Block, CMC and PHY

- **Dual sourcing of ESD protection uncritical**, because ESD protection in front of DC block and CMC protect whole system
- External ESD protection is decoupled from internal protection of the PHY. **PESD2ETH1G-T matches with every PHY**

100BASE-T1 concept comparison

Comparison of ESD protection concepts evaluated by EMI scanner

No Protection

Classic Protection

PHY

Classic ESD protection

Connector

OA compliant ESD protection

public

100BASE-T1 concept comparison

Comparison of ESD protection concepts evaluated by EMI scanner

No Protection

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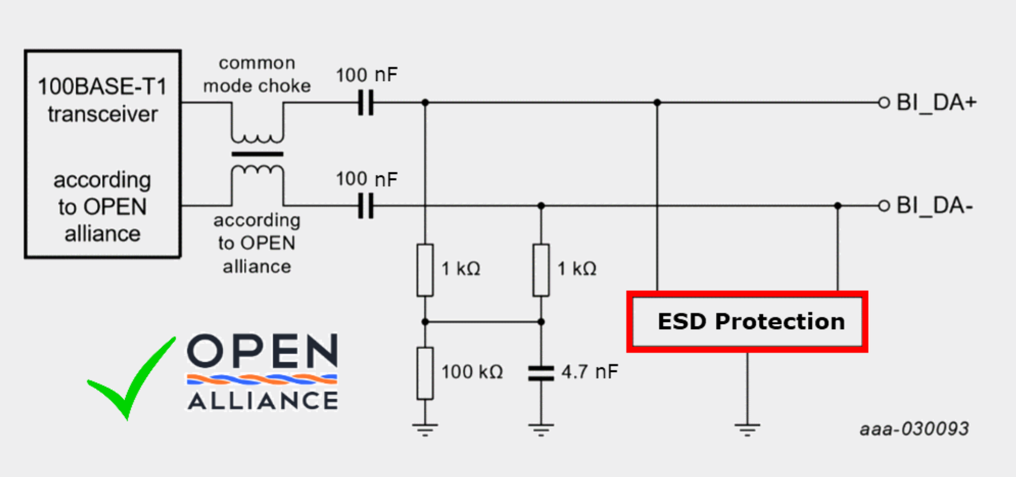
OPEN Alliance Spec. for ESD protection devices

General requirements



- **General requirements**
  - **Bi-direction device, 15kV IEC, 1000 discharges**
  - **Trigger voltage > 100V, $V_{DC,max}$ > 24V**
- Additional tests
  - Mixed mode S-parameter measurements
    - To evaluate transmission, symmetry, and mode conversion, replaces requirements on C_p and matching
  - Damage from ESD
    - To verify degradation, first measure S-parameters, apply ESD (8kV) discharges, and check S-parameters again

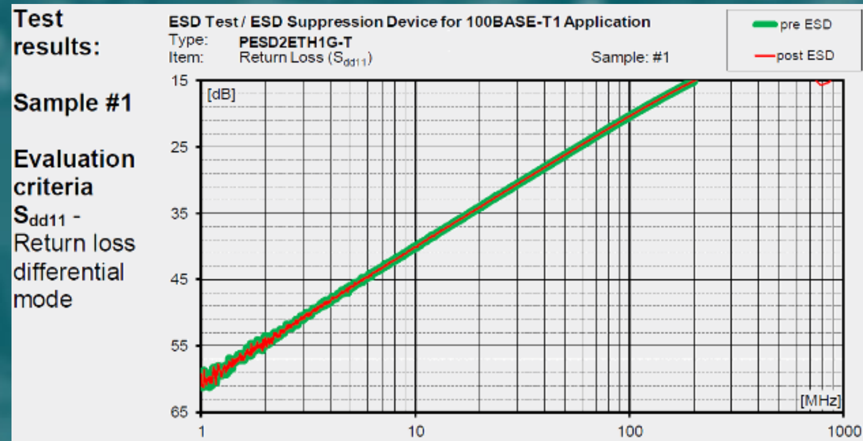
Signal Integrity

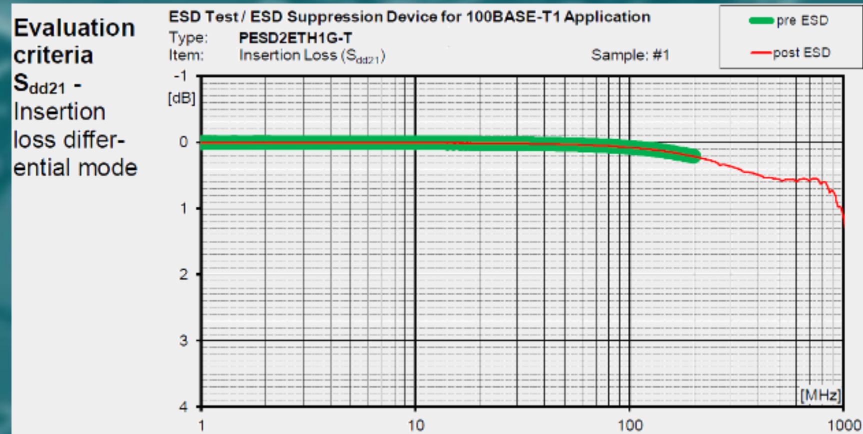
  - ESD discharge current measurement
    - Quantification of the current that would flow into the PHY

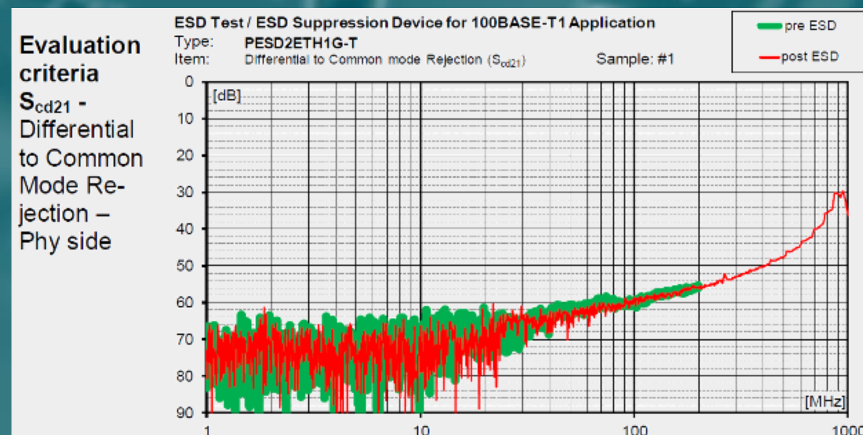
ESD, PHY

  - Unwanted clamping
    - Evaluate impact of ESD device onto RF immunity testing

Immunity







OPEN Alliance Spec. for ESD protection devices

Damage from ESD

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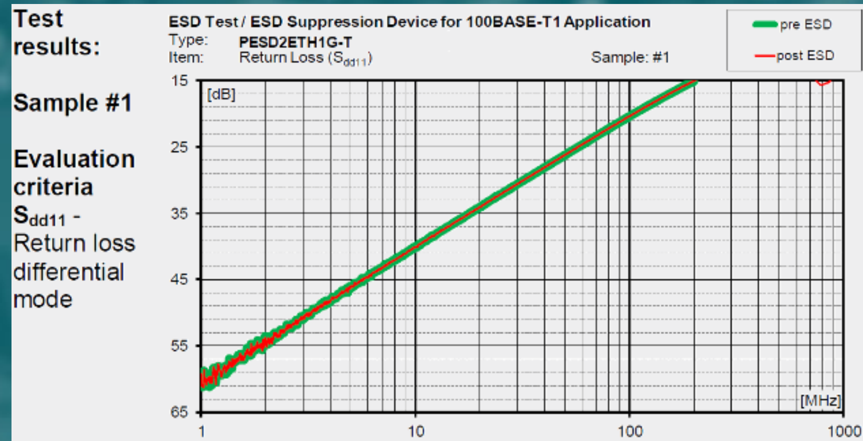

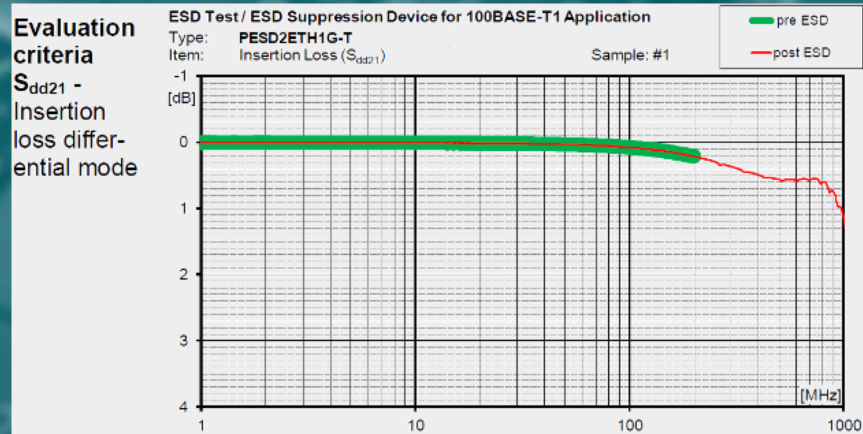

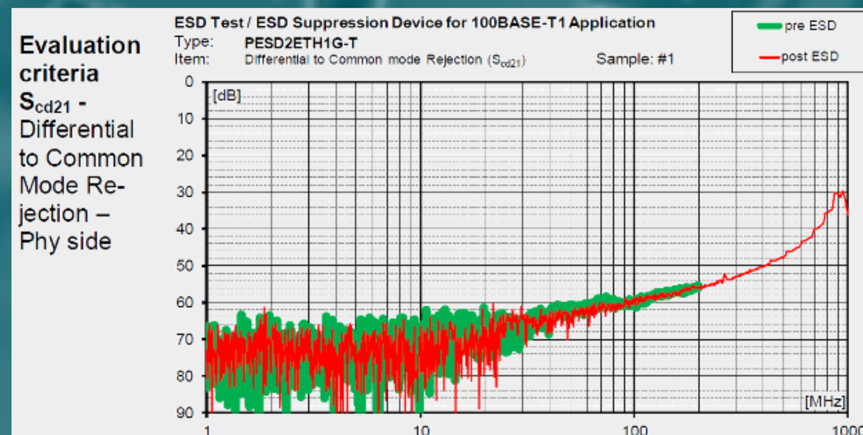

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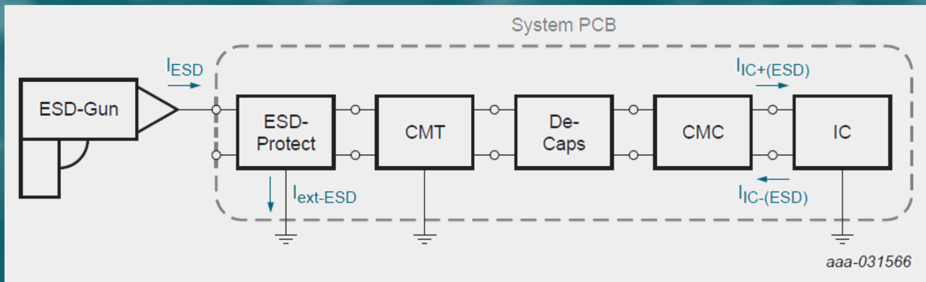

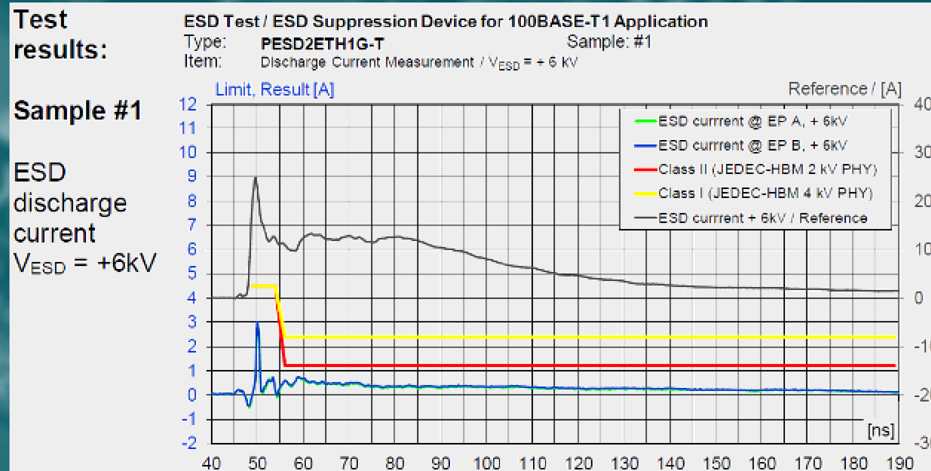

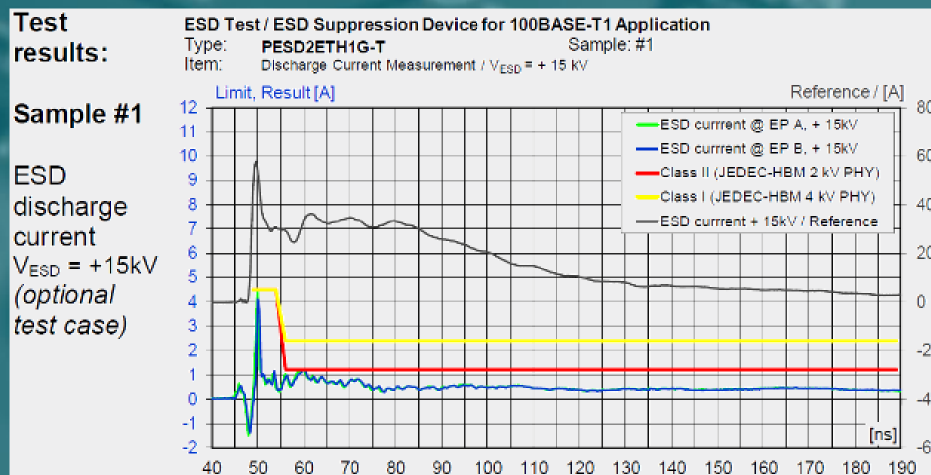

OPEN Alliance Spec. for ESD protection devices

ESD discharge current measurement

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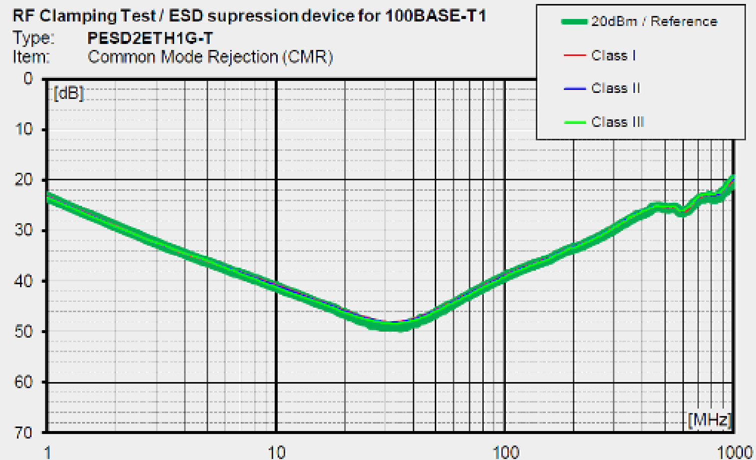
OPEN Alliance Spec. for ESD protection devices

Unwanted clamping



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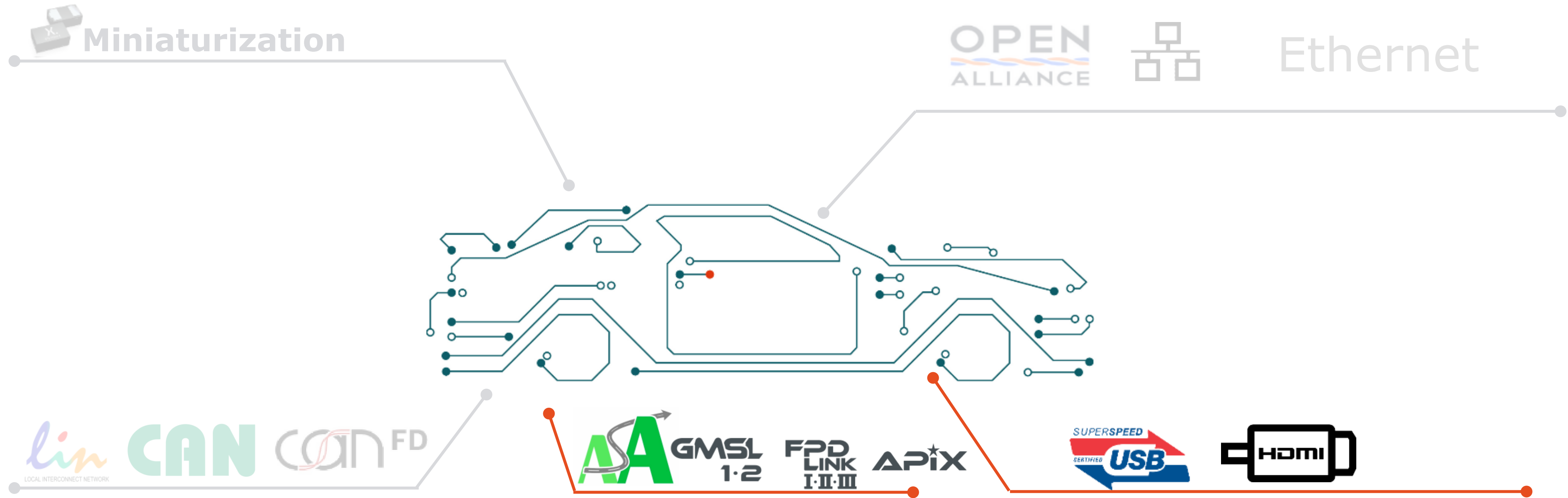
Automotive ESD Protection



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Challenges for High-Speed Interfaces

ESD

- >8kV (15kV)
- Different requirement on V_t and V_h
- Robust and reliable technology

Signal Integrity

- Small capacitance and other parasitics
- Routing
- Impedance
- S-parmeter (also MM)

EMC

- Emission (CE, RE)
- Immnity (RI, Stripl., BCI, etc.)
- Pulses (e-car?)

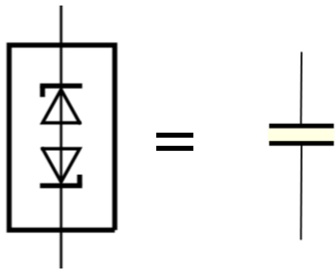
Automotive Environment

- Temperature
- Humidity
- Vibrations
- AC Coupling in STP
- HV (e.g 48V)
- ...

Semiconductor technology, HF analysis (S-Param, Eye Diagramm, TDR), ESD Simulation - SEED, High-Speed Packages

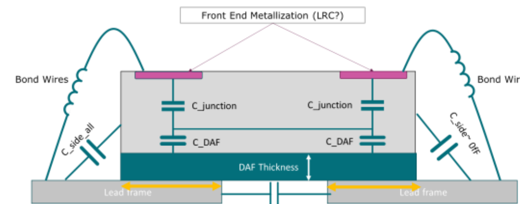
Parameters impacting Signal Integrity

Device Capacitance



- Semiconductor technology (SCR, open base, etc.)
- Capacitance matching

Package parasitics

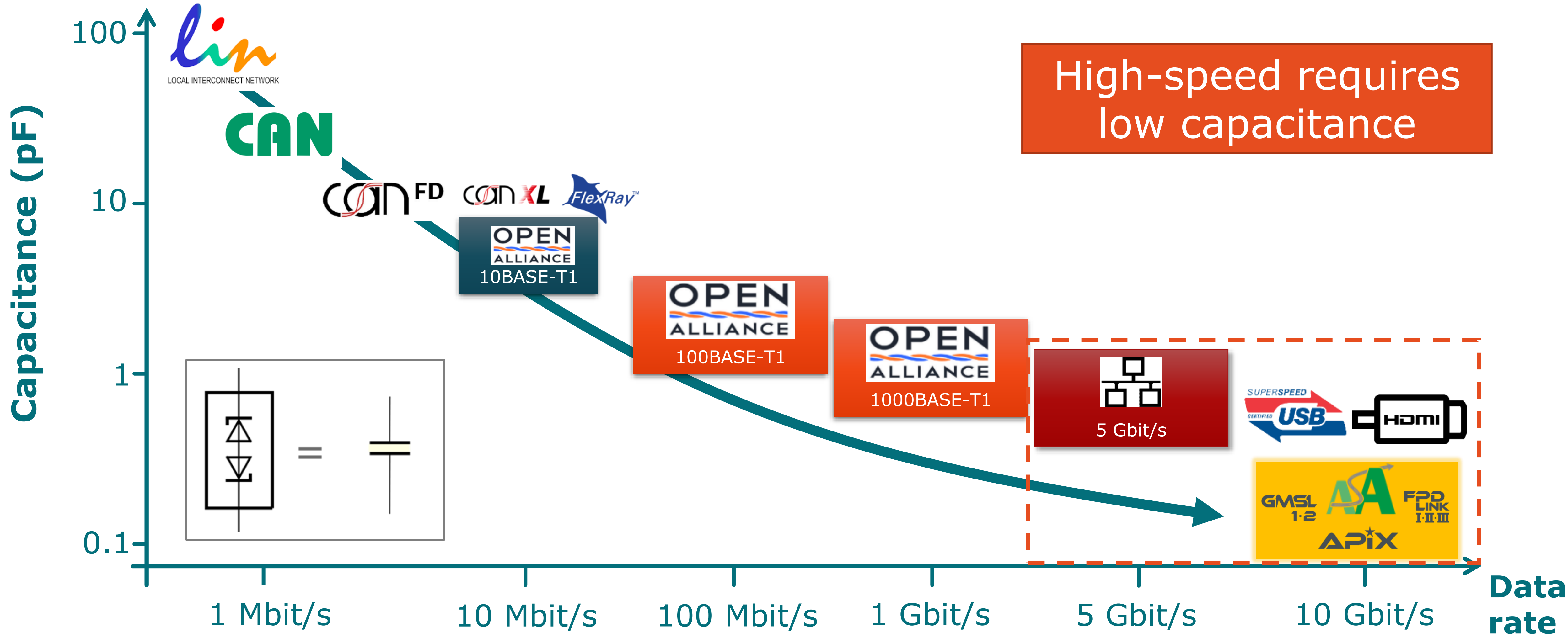


- Package technology
- Package size

Routing

- Impedance mismatch
- Assymetries
- Pad discontinuity

Application overview: capacitance vs. datarate



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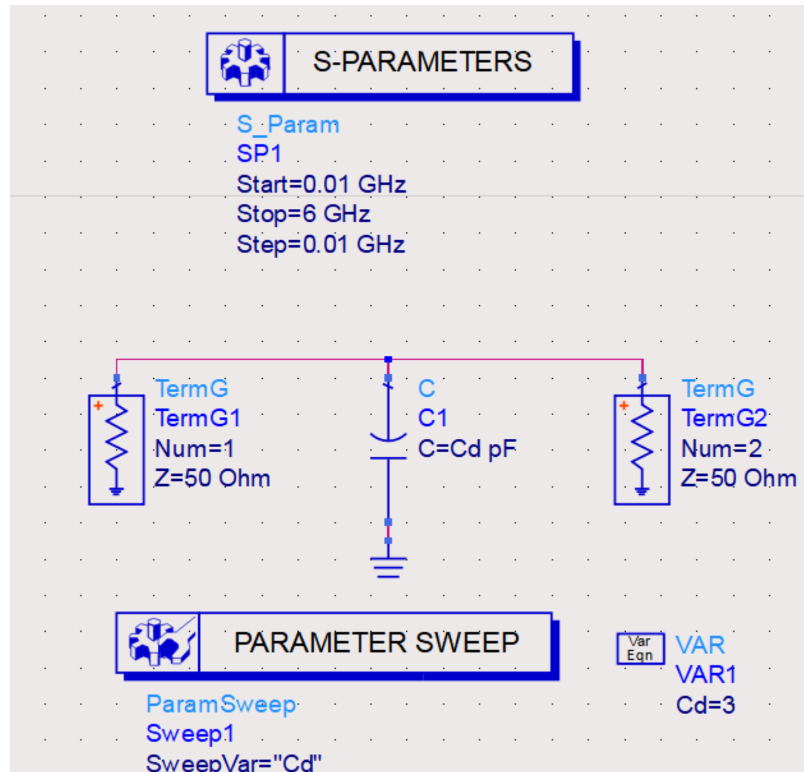
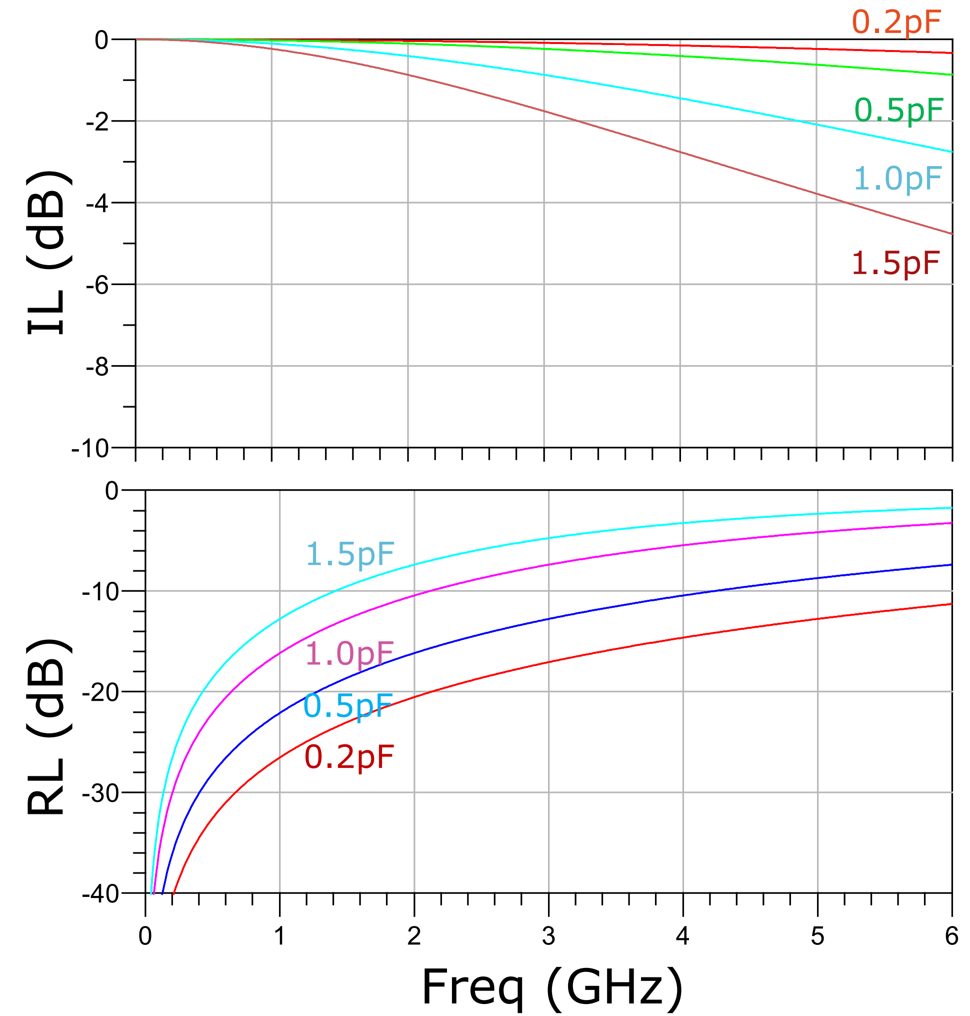
Impact of Capacitance

S-Parameters





ESD Protection Device

Measurement vs simulation of capacitor

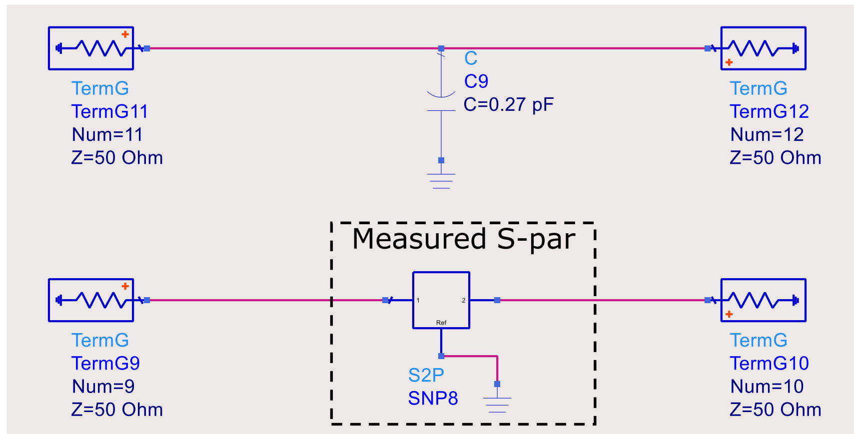
Nexperia — **PESD30VF1BL**

Bidirectional ESD protection diode

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	30	V
V_{BR}	breakdown voltage	I_R = 10 mA; T_{amb} = 25 °C		31	34	39	V
I_{RM}	reverse leakage current	V_R = 30 V; T_{amb} = 25 °C		-	0.1	50	nA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	0.27	0.4	pF
V_{CL}	clamping voltage	I_{PPM} = 1 A; T_{amb} = 25 °C	[1]	-	6.5	-	V
		I_{PP} = 16 A; T_{amb} = 25 °C	[2]	-	23	-	V
R_{dyn}	dynamic resistance	I_R = 7.5 A; T_{amb} = 25 °C	[2]	-	0.7	-	Ω



0.27pF simulation

measurement

|S-Par| (dB)

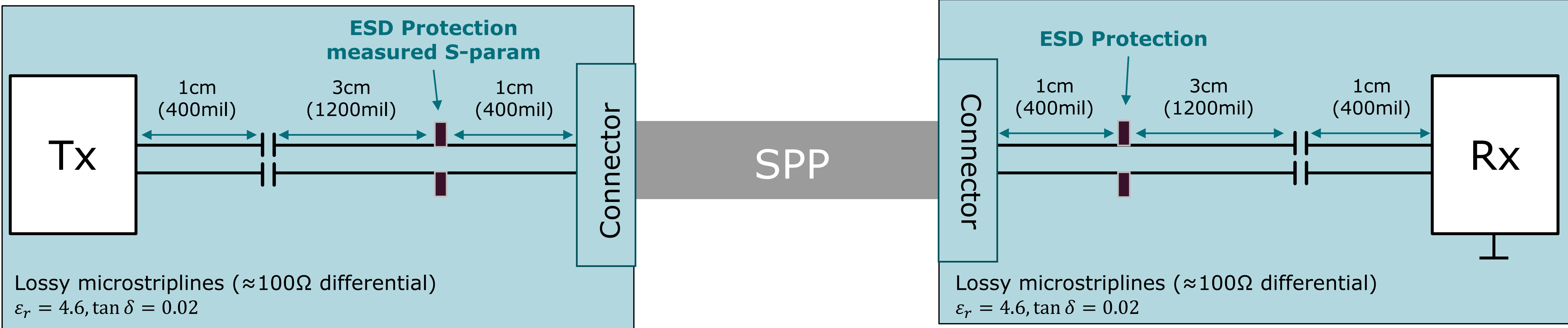
0
-10
-20
-30
-40

0 1 2 3 4 5 6 7 8

Freq (GHz)

Simulation of a High Speed Link

PHY – Cable - PHY

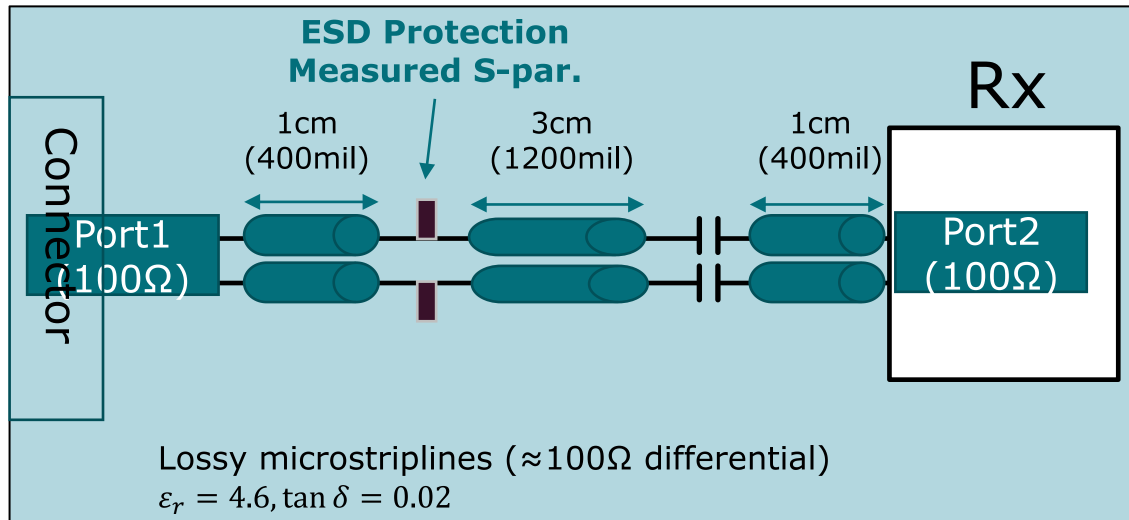


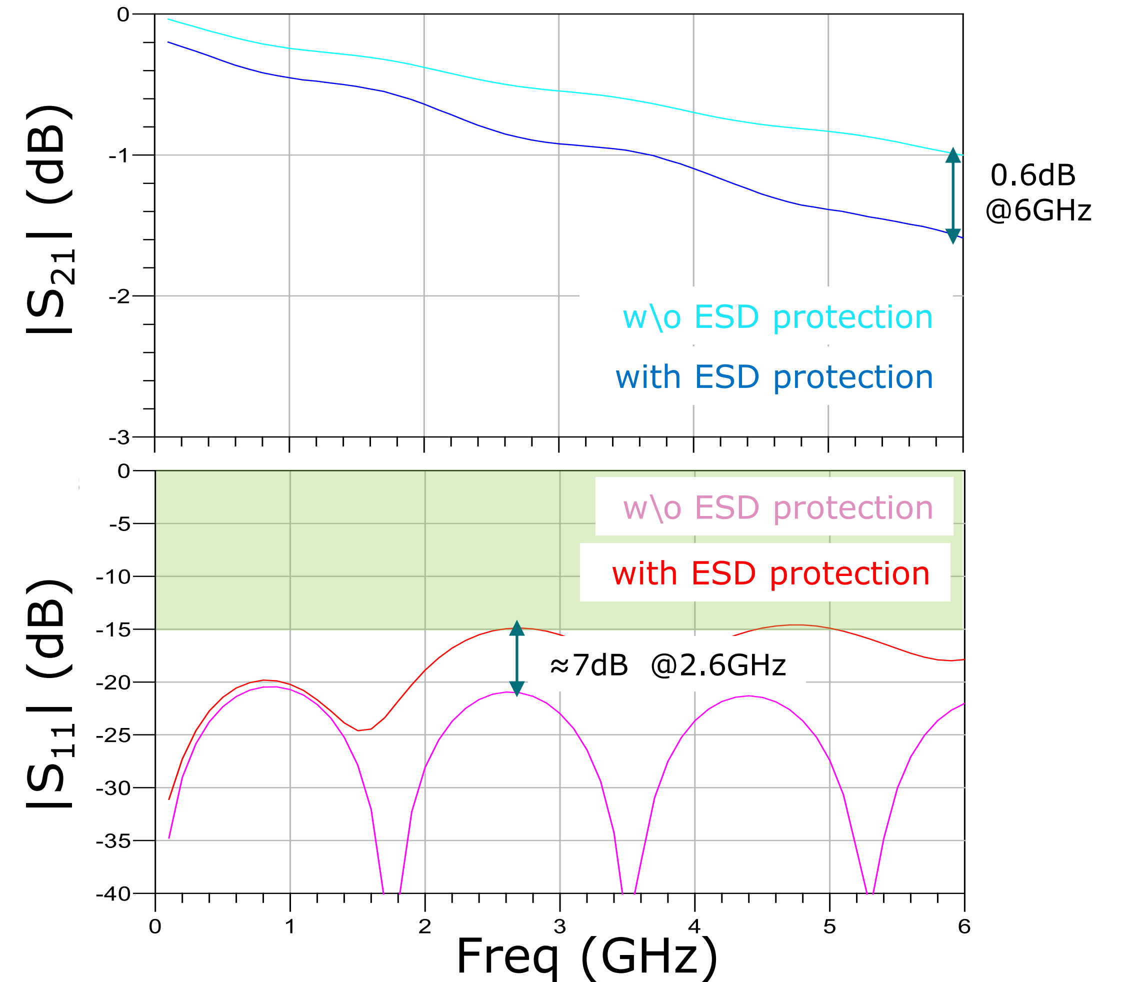
1. Simulate Rx/Tx system separately
2. Include cable
3. Include connector

public

Simulation of High Speed Links

S-parameters simulation in ADS

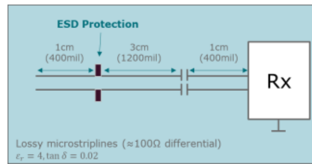


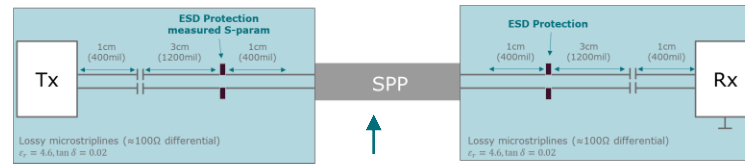


Ideal system, not including e.g. cable and connector!

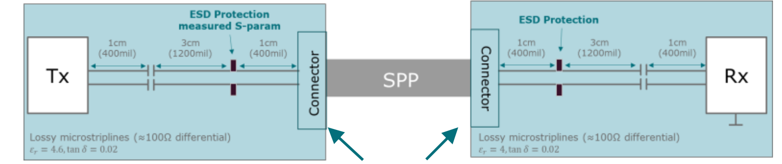
Simulation of a High Speed Link

PHY – Cable – PHY: Results

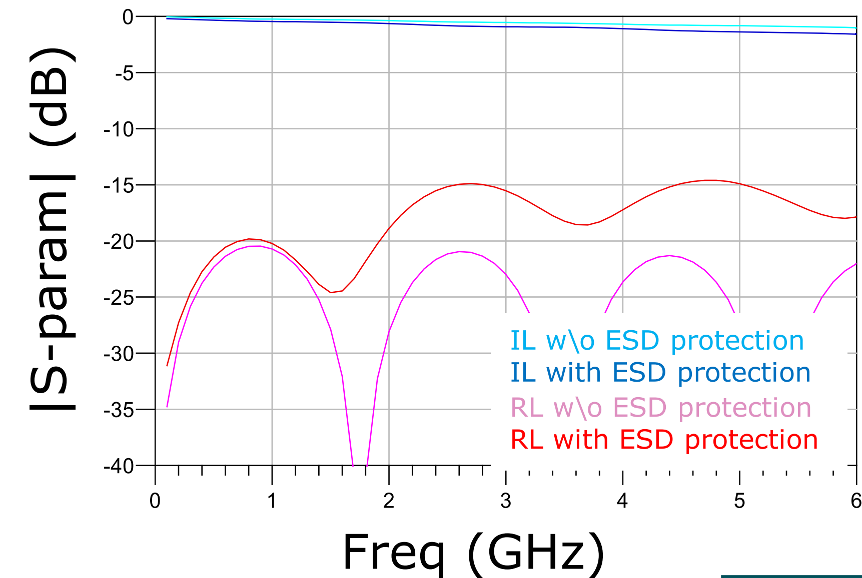


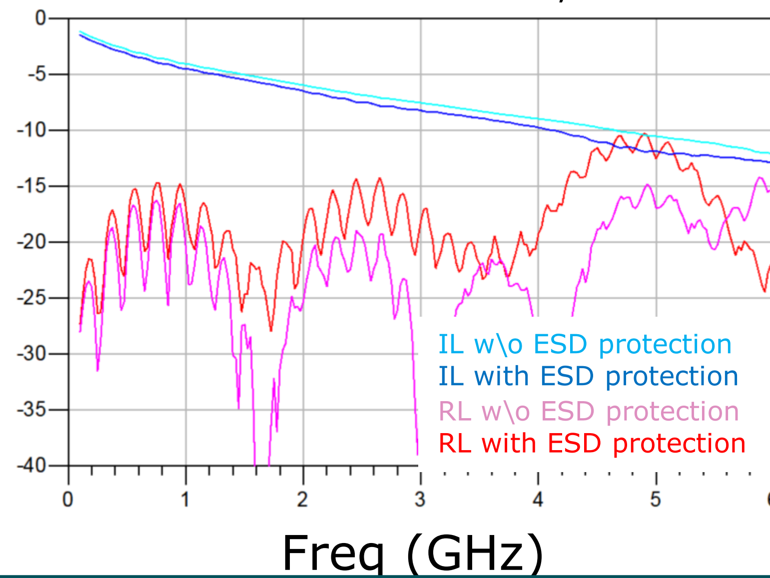


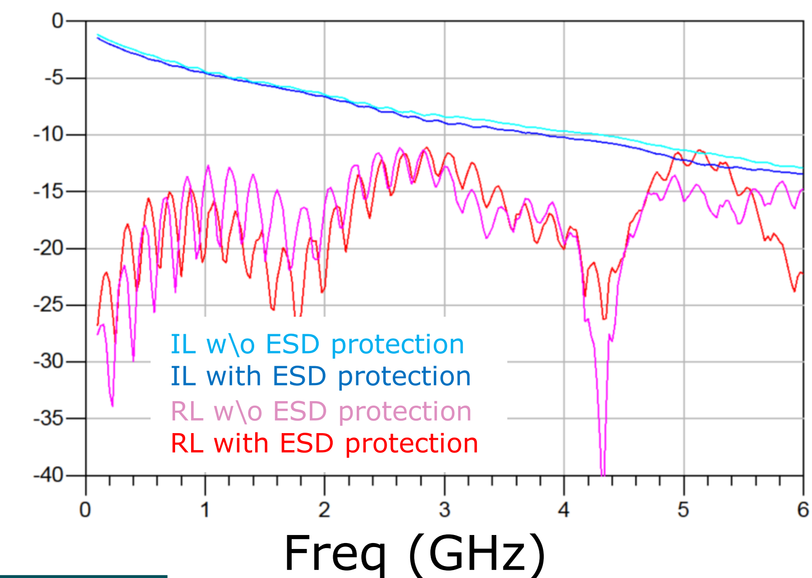
Measured S-Parameter, 10m



120Ω







Ideal

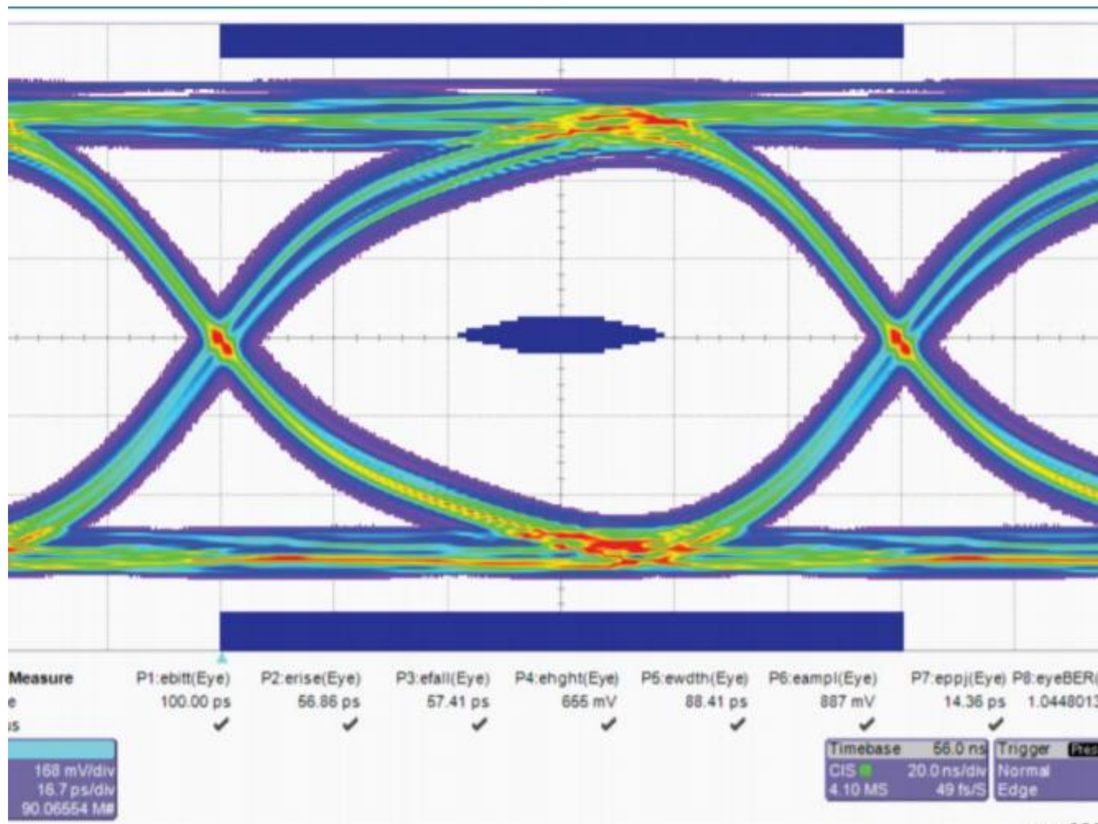
The more real the simulation the less impact can be observed from a modern ESD protection device.

Real

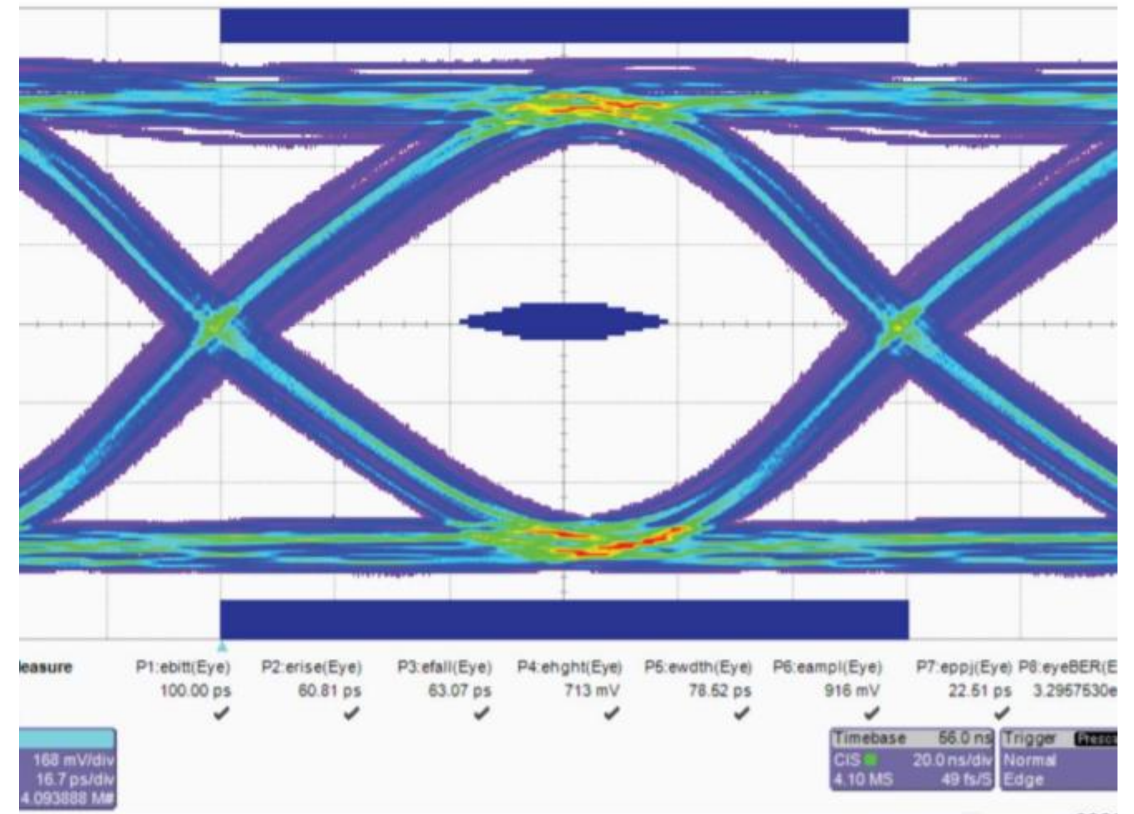
public

Signal Integrity

Eye Diagramm (Cd=0.17pF)



w/o ESD device



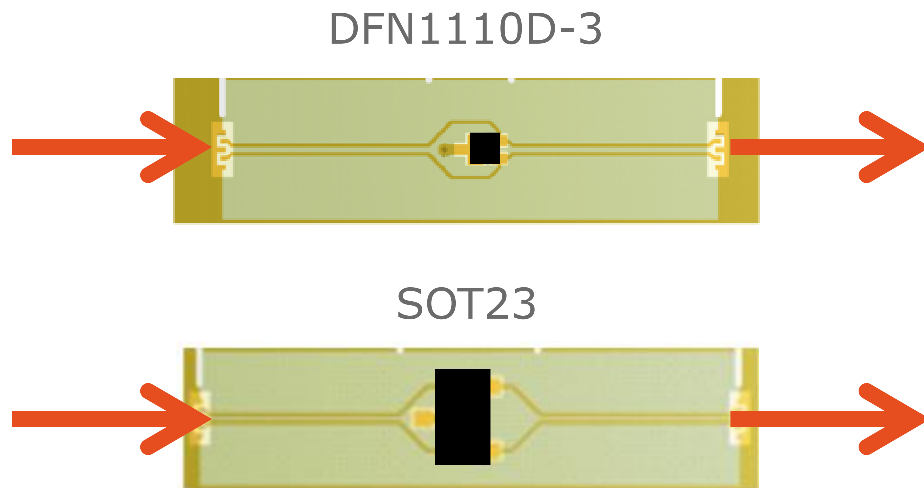
with ESD device

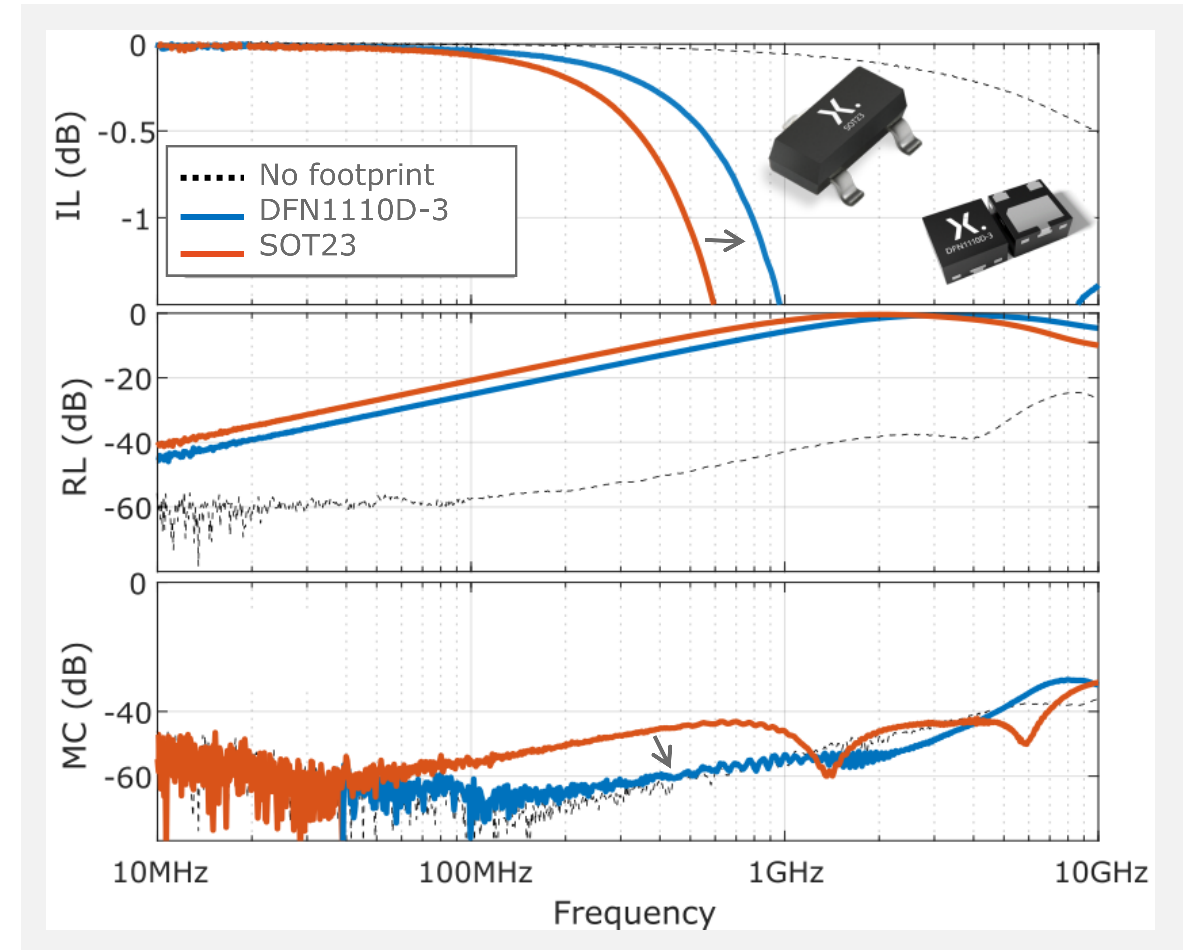
public

Package Aspects

Comparison of SOT23 and DFN1110D-3 with PESD2CANFD24Vx (C_d = 5.2 pF)

- Ca. 2 cm traces on FR4
- Dashed line: no footprint
- **Clear advantage of leadless package**





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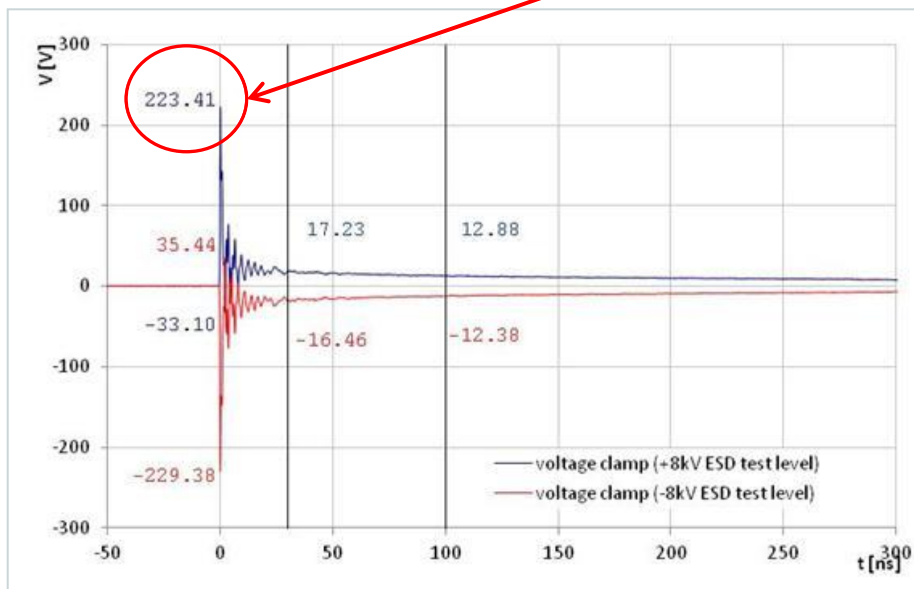
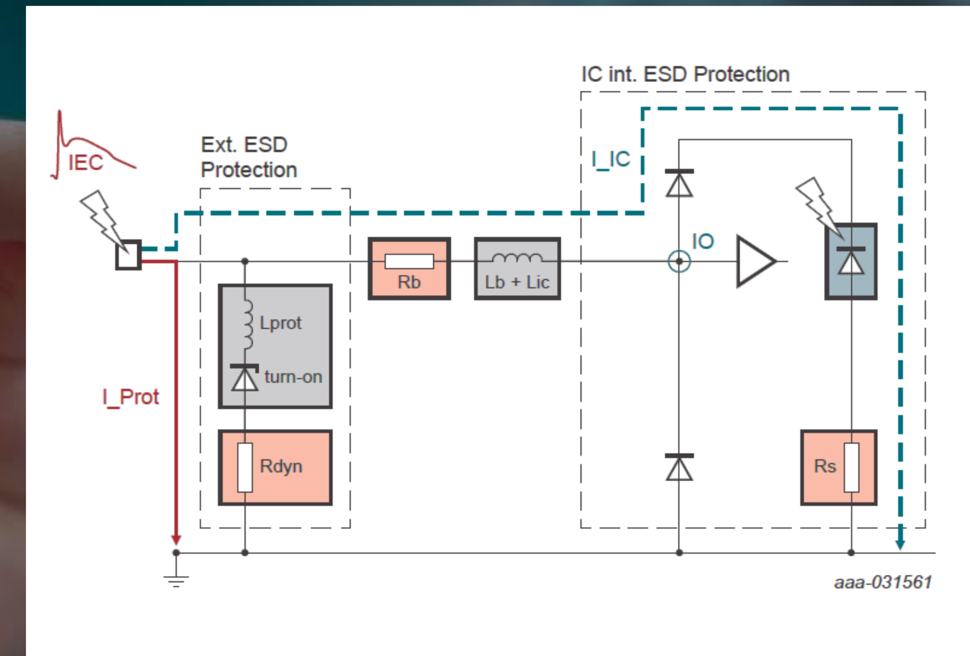
Package aspects – Clamping behavior

For high-speed busses

- Rdyn governs the clamping voltage in a quasi-static condition
- The dynamic behavior is determined by inductances and turn-on behavior





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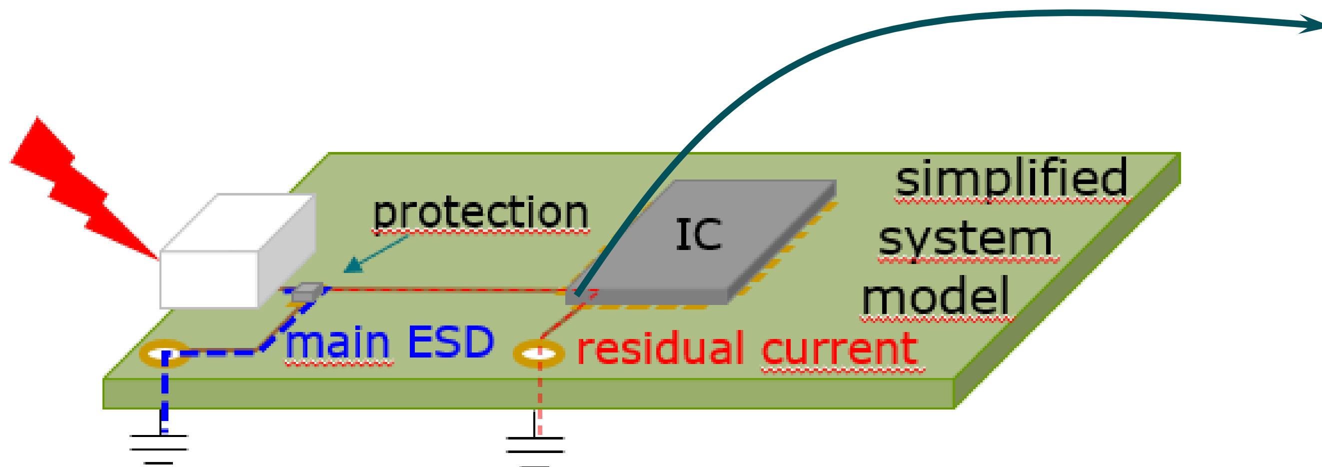
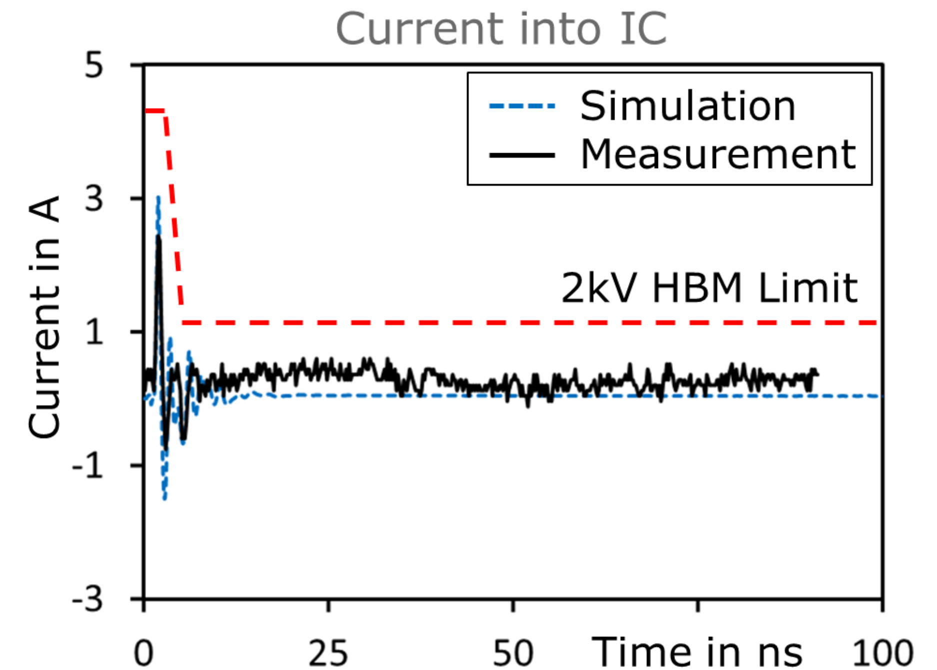
System Efficient ESD Design (SEED)

- SEED simulates residual currents and voltages at IC pins
- Dynamic models for ESD protection and common mode chokes for ADS and Spice
- **Allows to pick best protection during system concept design and significantly improve system robustness**





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Conclusion

- ESD can irreversibly distruct any electonic system, especially sensitive in-vehicle networks
- External ESD Protection can increase the system robustness of your system significantly
- ESD protection devices must be chosen for each application specifically
- Dedicated ESD protection can improve the system robustness of High-Speed applications without compromizing SI
- SEED simulations help to simplifiy the selection and design process

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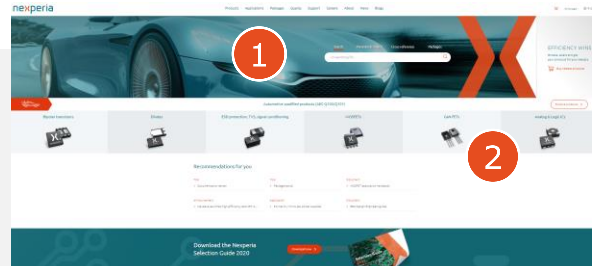

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(1)

- Product Overview
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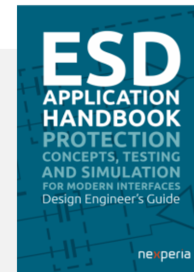
(2)

Documentation Center

Link Selection Guide

- Overview on all our Discrete, Logic and MOSFET devices
  - Diodes & Transistors
  - **Protection & Filtering**
  - MOSFETs
  - Logic
  - Packages



Application Handbook

Link ESD

- ESD Fundamentals
- Measurements & Characterization
- Interfaces and applications
- English & Chinese version
- PDF & Hardcopy

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EFFICIENCY WINS.